DESIGN OF HIGH-PERFORMANCE MAC UNIT USING LOW COMPLEXITY REVERSIBLE MULTIPLIER

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Abstract: In the real world of DSP(Digital Signal Processing), the MAC unit ie Multiply-Accumulate Computation holds a pivotal position within the critical processing path. Among its components, the multiplier stands out as a fundamental building block. The altogether performance of the multiply accumulate computation unit is intricately linked to the resources allocated to the multiplier. Hence, this paper proposes low complexity reversible multiplier, specifically engineered to enhance the power efficiency, delay and area of the multiplier. The Multiply-Accumulate Computation(MAC) unit, equipped with a multiplier employing this novel partial product reduction technique, yields significant improvements: a 46% reduction in delay, a 39% decrease in power consumption, and a 17% reduction in area requirements when collate to a MAC unit employing an architecture of a conventional multiplier.

Keywords: MAC Unit, Reversible Multiplier, DSP, Adders, Area, Delay, Power

I. INTRODUCTION

The multiply-accumulate operation is a fundamental operation within DSP architecture and finds widespread use. To compute expressions like:

$$y[n] = \Sigma\, x[k] * h\,[n - k] \quad (1)$$

Where before adding the productsyou need to multiply various values of x and h to obtain an output y[n]. Rather of hold on for the results of multiplication operations to set off accessible before performing addition, the MAC (Multiply-Accumulate) operation allows parallel computation of addition alongside multiplication. The hardware responsible for this is known as the MAC unit. The common expression exhibiting the Multiply-Accumulate operation is as follows:

$$y\,[n + 1] = y[n] + x\,[n + 1] * h\,[n + 1] \quad (2)$$

Here, x[i] is the multiplier, h[i] represent the multiplicand, each ofsize n-bit. The fundamental block diagram of the Multiply-Accumulate (MAC) unit is illustrated in Figure 1.

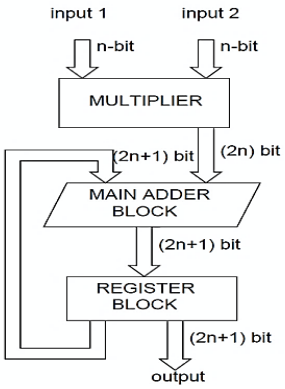

Figure - 1: Fundamental MAC Unit

The multiplication-accumulation operation stands as a central computational core and is regarded as a fundamental operation within the field of Digital Signal Processing [1]. The Multiply-Accumulate unit, an essential component for architecture of DSP, holds the key to the overall frameworks speed, as it typically resides in the critical processing path. The creation of a effective MAC unit holds immense significance for continuous DSP applications. Furthermore, in light of the accelerating demand for concise electronic devices, electronic components accompanied by moderate power utilization and minimal space requirements are imperative from a market perspective. As such, the design of a multiply-accumulate (MAC) unit accompanied by speedy performance, reduced area requirements, and moderate power utilization becomes a critical consideration inDSP systems and video coding in real-time[2].

To enhance the performance of the MAC-Multiply-Accumulate unit with regard to critical path delays and hardware complexity, there is a need to explore high-performance Multiplier-Accumulation units [3]. To achieve better power, delay, and speed performance in the MAC-Multiply-Accumulateunit, improvements in the multipliers performance parameter, that compose a dominant part of the Multiply-Accumulateunit, are essential. Substantial efforts have been directed towards developingdesigns andalgorithms of advanced multiplication[1]. Improvingperformance of multiplier involves reducing the assets used by theblock of partisan product reduction. Carry propagation can be stagnant, and within the same MAC-Multiply-Accumulate circuithaving

two distinct carry propagations is ineffective. Back to the input blockof the partial product reduction by feeding the multiplier output the particular issue could be addressed, reducing the requirement for a traditional accumulation adder[4], [5], [6]. Accumulation is then managed by the multipliers final adder, requiring just stage of a single carry propagation. It's important to note that this enhancement applies primarily to one cycle (MACs)Multiply-Accumulate, where in a lot of applications long critical delays are limiting factor.

The architecture of multiplier proposed in this paper is in compliance with a fundamental multiplication algorithm, akin to a traditional paper-pencil approach[7], and undergoes 3 key steps: 1) Partial Product generation, 2) Partial product reduction, 3) Final(carry-propagated) addition. The block of partial product reduction is the resource intensive, and to address this,circuits of parallel prefix which take n inputs and generate outputs came to be employed to fabricate effective adders[8], [9]. Those adders were utilize to implement the block of an imperfect product reduction, resulting with enhance performance in a multiplier[10].Therefore, this paper introduces a low complexity reversible multiplier, specifically engineered to enhance the multipliers power efficiency, area, and delay.

II. LITERATURE REVIEW

A literature review on the MAC-Multiply-Accumulate unit reveals a rich history and significant contributions in the fields of digital signal processing (DSP) and microprocessor architecture. The MAC unit enact a critical role in abundant applications like filtering, Fourier transforms, and various mathematical computations. Below is a concise literature review highlighting key findings and developments in the realm of MAC units:

Historical Perspective: The concept of the MAC unit dates back to the early days of digital computing. It was initially employed in analog computers and later integrated into digital systems. Over time, MAC units evolved to become a fundamental building block in modern microprocessors.

Role in Digital Signal Processing:MAC units are fundamental for DSP applications. They enable efficient execution of mathematical operations like convolution, filtering, and correlation, which are crucial in audio, image, and video processing.

Impact on Performance: Several studies have demonstrated that the efficiency of MAC units significantly influences the overall performance of DSP systems. Optimizing MAC unit design can lead to faster and more energy-efficient processing.

Parallelism and Pipelining: Research has focused on enhancing MAC unit performance through parallelism and pipelining techniques. These approaches aim to improve throughput and latency, making MAC units suitable for real-time signal processing.

Arithmetic Precision and Precision Scaling: Achieving high precision in MAC units is vital in many DSP applications. Researchers have explored techniques for accurate representation of real numbers and scaling to prevent overflows or underflows.

Custom MAC Units: Tailored MAC units have been developed for specific applications, like neural networks and deep learning. These custom MAC units optimize hardware resources and maximize computational efficiency.

Low-Power MAC Units: With the growing demand for energy-efficient devices, numerous studies have focused on designing low-power MAC units. Techniques include voltage scaling, algorithmic optimization, and reduced arithmetic precision.

FPGA-Based MAC Units:FPGA implementations of MAC units have gained attention for their flexibility and reconfigurability. Researchers have explored FPGA-based MAC units in various signal processing applications.

Novel Algorithms and Architectures: Researchers have introduced novel algorithms and architectures for MAC units, addressing specific challenges and optimizing performance. These innovations have the potential to reshape the field of DSP.

Numerous endeavours have been made to create low-complexity reversible multipliers, as evidenced by references [11-22] in recent research. While these developments exhibit variations, they share several common characteristics.Primarily, they are designed by translating the fundamental components of traditional multiplication structures (e.g: half adders and full adders) into Reversible Logic (RL) gates. In table-1, we can observe quantum cost (QC), quantum implementation, and logic symbols for several commonly utilized reversible gates in existing reversible multipliers. Notably, any addition circuit could be constructed from the multiplexers, and with a 3x3 reversible Fredkin gate each multiplexer can be substituted, occasionally with P and R outputs left unused.Where this accession eases design of hierarchical to a certain scope, it results in a proliferation of gates and superfluous outputs, which can lead to circuit layout congestion.

Table - I: Logic Symbols

Gate	Logic symbol	Quantum implementation	QC
Feynman [18]	A, B — FG — P=A, R=A⊕C	A — A; B — A⊕B	1
Double Feynman [18]	A, B, C — F2G — P=A, Q=A⊕B, R=A⊕C	A — A; B — A⊕B; C — A⊕C	2
Peres [19]	A, B, C — PG — P=A, Q=A⊕B, R=AB⊕C	A — A; B — A⊕B; C — AC⊕B	4
Toffoli [3]	A, B, C — TG — P=A, Q=A⊕B, R=AB⊕C	A — A; B — B; C — AB⊕C	5
Fredkin [20]	A, B, C — FRG — P=A, Q=A'B⊕AC, R=A'C⊕AB	A — A; B — A'B⊕AC; C — A'C⊕AB	5
Double XOR [8]	A, B, C, D — BVF — P=A, Q=A⊕B, R=C, S=C⊕D	A — A; B — A⊕B; C — C; B — C⊕D	2
HNG [11]	A, B, C, D — HNG — P=A, Q=B, R=A⊕B⊕C, S=(A⊕B)C⊕(A⊕B)D	A — A; B — B; C — A⊕B⊕C; B — (A⊕B)C⊕(A⊕B)D	6

III.PROPOSED MAC UNIT WITHLOW COMPLEXITY MULTIPLIER

A standard MAC (Multiply-Accumulate) unit with n bits typically comprises a multiplier of n-bit, an adder of 2n-bit, and an accumulator of 2n-bit. Different Multiply-Accumulate unit configurations can created by substituting thecomponent of multiplier with diverse architectural alternatives. The figure-2 below shows the proposed MAC unit with proposed low complexity reversible multiplier.

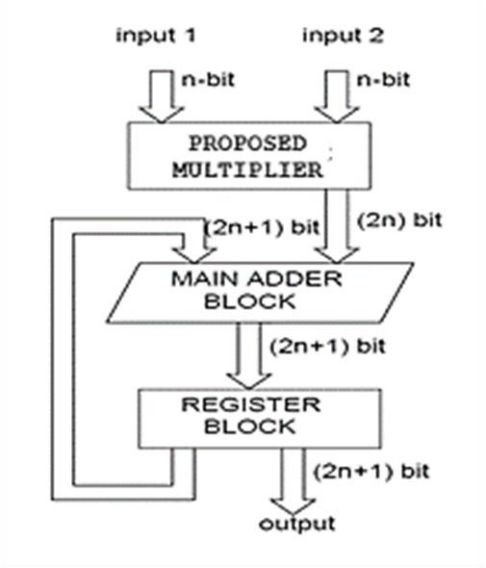

Figure-2: Proposed MAC Unit with proposed low complexity reversible multiplier

Proposed Low Complexity Reversible Multiplier

The figure -3 employs PG and HNG reversible gate logic to implement proposed low complexity reversible multiplier. This circuit offers notable advantages when compared to the circuits.Therefore, the least complex reversible addition array must incorporate the PG based Half-Adder and singular gate realization of a Full-Adder. As depicted in Figure -3, an instance of the most cost-effective reversible implementation of an addition array utilizes the HNG gate as the Full-Adder component. This circuit comprises 12-gates, 12-fixed inputs, 20-extraneous outputs, and have a quantum-cost of 64.

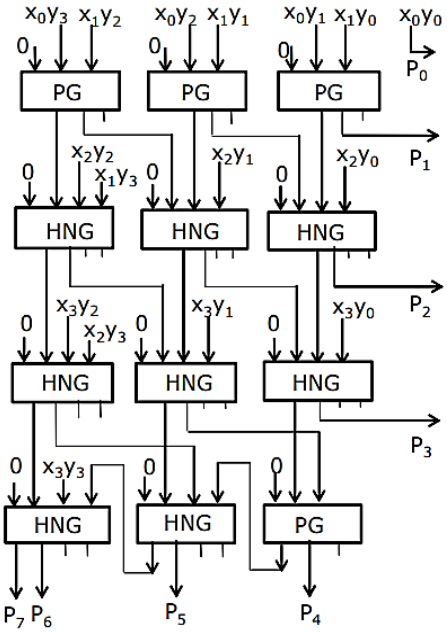

Figure - 3: Proposed multiplier

IV.EXPERIMENTAL RESULTS

Using Verilog Hardware Description Language both the subsist and proposed Multiply-Accumulate unit models were developed. The synthesis and simulation processes, as detailed in [23], are conducted utilizing Xilinx ISE 13.2, targeting the device Virtex-6 family equipped with the 40nm CMOS technology.In the results of simulation, the Technology view [24] presents a schematic representation of the design optimized for the specific Xilinx device or technology. It focuses on logic elements tailored to the target, including Look-up-Tables (LUTs) [25],I/O buffers, carry-logic, and other components of technology-specific.On the other hand, a schematic representation offered by the RTL view of the pre-optimized design, depicted using inclusive symbols which remain individualistic of the earmarked Xilinx device. This view encompasses elements such as multipliers, AND gates, adders, counters, and OR gates.By creating a program of test bench the timing waveform is induced that includes a set-of input test vectors put-in to the design. This helps assess the design's performance and functionality. Figure-4 shows the schematic of technology view for the proposed MAC unit and Figure-5 shows the Proposed Multipliers Simulation Waveforms.

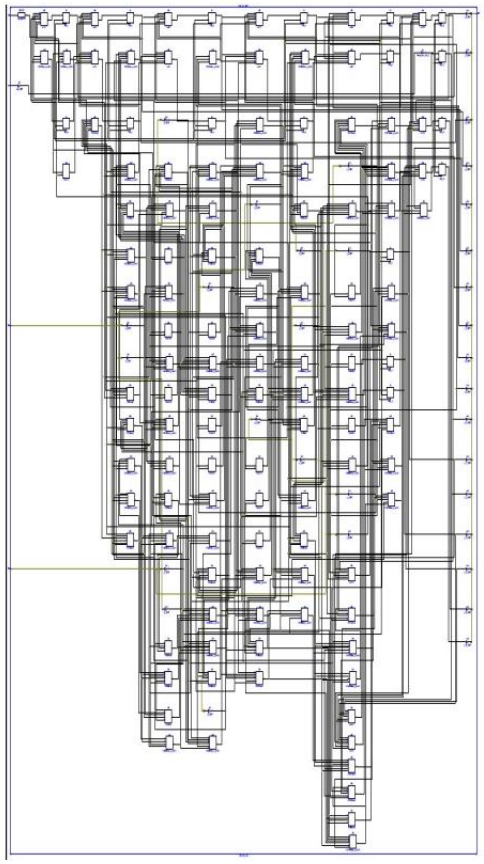

Figure - 4: Proposed MAC Units Technology View

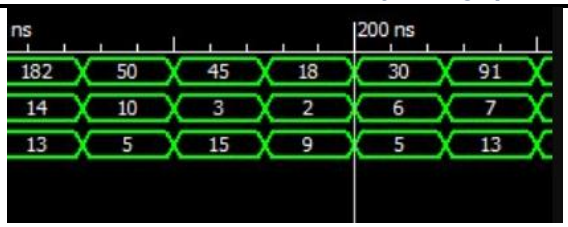

Figure - 5: Simulation Waveforms of Proposed Multiplier

Table-I shows the proposed MAC unit performance analysis with proposed and other multipliers.

Sl. No.	Design	Area (LUT's)	Delay (ms)	Power (W)
1	MAC with Proposed Multiplier	92	6.102	1.010
2	MAC with Wallace Tree Multiplier	96	6.712	1.061
3	MAC with Dadda Multiplier	103	6.810	2.142

V.CONCLUSION

In this paper,Multiply-Accumulate (MAC) unit model is crafted by Verilog Hardware Description Language (HDL), subjected to synthesis and simulation via Xilinx ISE 13.2, utilizing Virtex-6 40nm technology. The observation revealsthe model of proposed MAC unit, incorporating the novel, low-complexity reversible multiplier, outperforms existing models in both area and delay metrics. Furthermore, this endeavour can be expanded to encompass the design of MAC units with larger bit-sizes, like 16, 32, and 64, as well as for various applications like Arithmetic Logic Units (ALUs), filters, and more.

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