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An Accurate 2D Analytical Model for Transconductance to Drain Current ratio (g_m/I_d) for a Dual Halo Dual Dielectric Triple Material Cylindrical Gate All Around MOSFET

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A B S T R A C T

A dual-halo dual-dielectric triple-material cylindrical-gate-all-around/surrounding gate (DH-DD-TM-CGAA/SG) MOSFET has been proposed and an analytical model for the transconductance-to-drain current ratio (TDCR) has been developed. It is verified that incorporation of dual-halo with dual-dielectric and triple-material results in enhancing the device performance in terms of improved TDCR. The effect on TDCR is analyzed for variations in device parameters like oxide thickness, silicon thickness, channel doping concentration, channel length and drain bias.The results show that larger value of g_m/I_d can be obtained in proposed device in comparison to other existing triple material structures which makes it suitable for micropower applications. The analytical results of the developed g_m/I_d model strongly agrees with the simulated results obtained from TCAD Silvaco.

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NOMENCLATURE

q	Electronic charge	$t_{oxeffdh}$	Oxide thickness (nm)
N_{ak}	Acceptor ion concentration (atoms/m^3)	**Greek Symbols**	
$C_{oxeffdh}$	Oxide capacitance (F)	$\phi_k(r,z)$	Surface Potential (V)
R	Radius of silicon pillar (nm)	ε_{Si}	Permitivity of silicon
V_{fbk}	Flat-band voltage (V)	ϕ_{mk}	Work function of metal (eV)
E_g	Energy band gap (eV)	χ_s	Elecron affinity (eV)
g_m	Transconductance (mho)	ϕ_{fp}	Fermi potential (eV)

1. INTRODUCTION

At present conventional MOSFET has reached its scaling limit due to the presence of short channel effects and hence has degraded the device performance.So future generation devices require new device structures with new materials to accelerate the performance of device in nanoregime. The TM-SG MOSFET is the most popular device as compared to the planar MOSFETs [1]. Higher current driving capability, enhanced immunity against short channel effects, higher reliability and increased device packing density have been reported by many authors on this device [2, 3]. TDCR is a key metric to access the performance of a device instead of transconductance which is also known as the quality factor of a MOSFET device [4]. This ratio for the MOSFET device means the amplification produced by the device to power dissipated through drain current. The higher value of TDCR will give

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highest voltage gain of a MOSFET device which is necessary for analog/RF applications and also useful for designing of memory circuits [5, 6].

The surface potential technique to find the TDCR and body factor (n) of fully depleted double-gate SOI MOSFETs is presented by Rajendran et al. [7]. Kranti et al. [8] have sucessfully applied the analytical model to enhance the TDCR (g_m/I_d) of a vertical surrounding gate MOSFET. But this model cannot be applied to triple material surrounding gate devices. Balamurgan et al. [9] have proposed a TDCR model for DM-SG MOSFET. Ghosh et al. [10] developed a model for dual material dual dielectric CGAA MOSFET. But not useful for triple material dual dielectric MOSFETs. Wang et al. [11] have proposed a new structure known as TM-SG MOSFET in which the surface potential model was developed using superposition method. But the method comprises of complex mathematical equations. Recently a model was reported by Dhanaselvam et al. [12] for Triple material surrounding gate MOSFETs. The solution of Poisson equation gives TDCR. No work has yet been reported on the g_m/I_d ratio for DH-DD-TM-CGAA MOSFET.

In this paper, analytical model of TDCR is presented. The TDCR of proposed device is calculated by taking the derivative of minimum surface potential. Furthermore the effet of variation in device parameters like oxide thickness, channel length anddrain bias are also studied. The result revals that proposed device have more TDCR in comparison to existing TM-SG MOSFETs. The analytical results have been validated by simulated results with the help of TCAD Silvaco. Therefore, device geometry is a key parameter for designing of future VLSI circuits.

2. DEVICE STRUCTURE

Figure 1 shows the schematic diagram of DH-DD-TM-CGAA MOSFET structure.

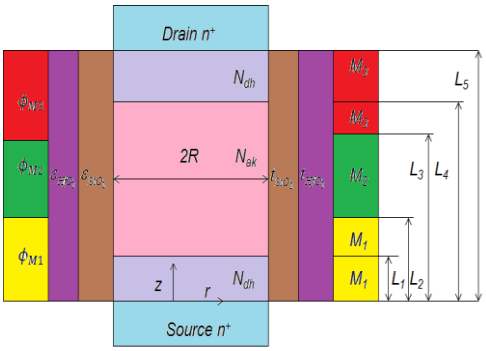

Figure 1. Cross sectional schematic of dual-halo dual-dielectric triple-material cylindrical-gate–all-around (DH-DD-TM-CGAA) MOSFET

Figure 1 shows that the gate terminal consists of three metals with different work functions for cylindrical surrounding gate MOSFET [13]. In this Triple metal gate schematic, the symmetric dual halo doping is incorporated for the first time along with dual dielectric to form a novel device structure. The lengths L_1 and L_5–L_4 are halo doped with concentration N_{dh} while the rest of the regions are doped with acceptor doping concentration N_{ak}, assuming that N_{dh} is greater than N_{ak} [14].

The cylindrical coordinate system is a radial direction *r*, an angular direction θ in the radial plane, and a vertical direction z, as shown in Figure1.The quantum effects are neglected in the present analysis as the device diameter and channel length is not below 10 and 30 nm, respectively [15].

The potential distribution in the channel can be expressed by the Poisson's equation [16] and can be written as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial[\phi_k(r,z)]}{\partial r}\right)+\frac{\partial^2[\phi_k(r,z)]}{\partial z^2} = \frac{qN_{ak}}{\varepsilon_{Si}}\left(L_{k-1}\le z\le L_k\right) \quad (1)$$

where, k=1, 2, 3, 4, 5

The total potential for the entire channel length can be defined as:

$$\phi(r,z)=\begin{cases}\phi_1(r,z);0\le z\le L_1\\ \phi_2(r,z);L_1\le z\le L_2\\ \phi_3(r,z);L_2\le z\le L_3\\ \phi_4(r,z);L_3\le z\le L_4\\ \phi_5(r,z);L_4\le z\le L_5\end{cases} \quad (2)$$

The potential distribution is approximated using parabolic profile for DH-DD-TM-CGAA MOSFET in the radial direction and is given by literature [10].

$$\phi(r,z)=\zeta_0(z)+\zeta_1(z)r+\zeta_2(z)r^2 \quad (3)$$

Were, the constant $\zeta_0(z)$, $\zeta_1(z)$ and $\zeta_2(z)$ can be obtained by substituting conditions at the boundary.

For obtaining surface potential, the corresponding boundary conditions are also reported in literature [17]: Using the boundary condition equations, in the surface potential Equation (3) and then substituting in Equation (1). Surface potential is expressed as follows:

$$\frac{d^2\phi_s(z)}{dz^2}-\phi_s(z)\left(\frac{2C_{oxeffdh}}{\varepsilon_{Si}R}\right)+(v_{gs}-v_{fbk})\left(\frac{2C_{oxeffdh}}{\varepsilon_{Si}R}\right)=\frac{qN_{ak}}{\varepsilon_{Si}} \quad (4)$$

$$\frac{d^2\phi_s(z)}{dz^2}-\kappa^2\phi_s(z)=\chi \quad (5)$$

$$\kappa^2 = \frac{2C_{oxeffdh}}{\varepsilon_{Si}R}, \chi = \frac{qN_{ak}}{\varepsilon_{Si}} - \kappa^2(v_{gs} - v_{fbk}) \tag{6}$$

where, k=1, 2, 3, 4, 5

$$v_{fbj} = \phi_{mj} - \left\{\chi_s + E_g - q\phi_{fp}\right\} \quad \text{where } j = 1,2,3,4,5 \tag{7}$$

The solution of second order differential Equation (5), through the complementary and the particular integral functions is given as:

$$\phi_{sk}(z) = \alpha_k e^{(\kappa z)} + \beta_k e^{(-\kappa z)} - \frac{\chi_k}{\kappa^2} \qquad l_{k-1} \le z \le l_k$$
$$M_k = \frac{\chi_k}{\kappa^2}, \delta_k = \exp(\kappa L_k), \delta_k^{-1} = \exp(-\kappa L_k) \tag{8}$$

where, α_k & β_k are arbitrary constants, which are calculated with the help of continuity conditions for the surface potential distribution (ϕ) and the field distribution (E) at the interfaces of different metal gates. For the value of α_k & β_k reported in literature [17].

The minimum surface potential is obtained by differentiating surface potential Equation (5) relative to the direction z and making it zero for getting the minimum surface potential ϕ_{s1min}.

$$\phi_{s1min} = 2\sqrt{\alpha_1\beta_1} - \frac{\chi_1}{\kappa^2} \tag{9}$$

The TDCR is a measure of the efficiency of the device. Hence it is also known as Transconductance generation efficiency or Transconductance generation factor. It is inversely proportional to thermal voltage. The expression for TDCR is given as:

$$\frac{g_m}{I_{ds}} = \frac{q}{k_B T}\left(\frac{\partial\left(2\sqrt{\alpha_1\beta_1} - \frac{\chi_1}{\kappa^2}\right)}{\partial V_{gs}}\right) \tag{10}$$

3. RESULTS AND DISCUSSION

In order to scrutinize the effectiveness of the proposed model, the DH-DD-TM-SG and TM-SG MOSFETs devices were studied, compared and results are presented. Further, the DH-DD-TM-SG device outcomes were compared with the simulated results of ATLAS 3D device simulator. The simulation parameters for TDCR model analysis are: R=10nm, V_{gs}=0.2V, $t_{oxeffdh}$=2nm. The work function of metal gate at the source end is 4.8 eV (Au) and work function of metal gate at the drain end is 4.4 eV (Ti).

The TDCR is plotted with respect to the position along the channel length for diverse values of channel doping concentration are depicted in Figure 2. The increase in TDCR is observed with increase in the channel doping concentration. It is obvious from the figure that, larger the channel doping concentration more is the g_m/I_d ratio at a specific channel length. The analytical results are plotted and validated with simulated results obtained from TCAD Silvaco [18].

In Figure 3, the TDCR is plotted with respect to position along the channel length at different radius of silicon pillar. As the radius of silicon pillar increases, the g_m/I_d ratio decreases. It is observed from the figure that DH-DD-TM-CGAA MOSFET having higher g_m/I_d ratio at R=10nm. The analytical results have been compared with the simulated results using TCAD Silvaco and an excellent agreement was achieved between the two.

Figure 4 shows the variation in TDCR as a function of the position along the channel length at different drain bias. As channel length increases, g_m/I_d approaches its ideal value of q/KT, whereas for shorter lengths influence of short channel effects (SCEs) is more and g_m/I_d decreases significantly.

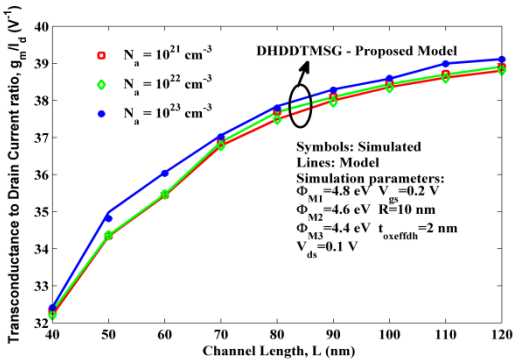

Figure 2. TDCR with varying channel length at different doping concentration

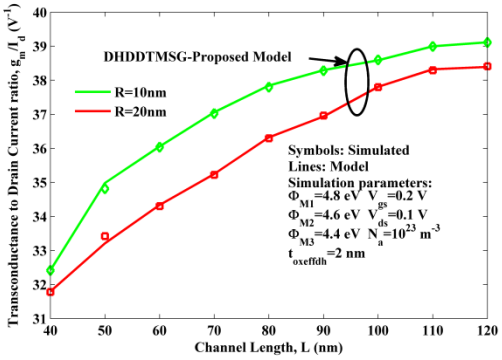

Figure 3. TDCR with varying channel length at different radius of silicon pillar

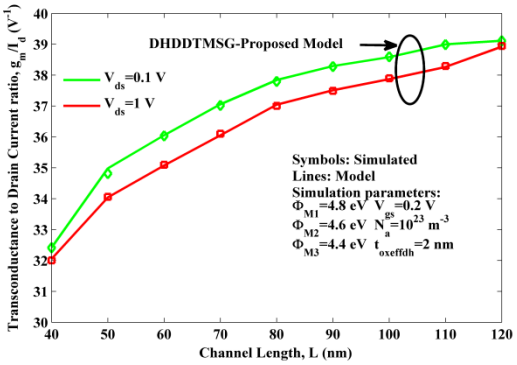

Figure 4. TDCR as a function of the position along the channel length at different drain bias for DH-DD-TM-CGAA MOSFET

It is also depicted in the figure that more value of g_m/I_d is achieved at lower value of V_{ds}. The abrupt reduction in g_m/I_d ratio at a particular value of channel length shows the starting of SCEs. The g_m/I_d decreases with the increase in drain bias and it is due to drain induced barrier lowering known as short channel effects. The DH-DD-TM-CGAA MOSFET have higher g_m/I_d at particular drain bias. The analytical results are plotted and validated with simulation result obtained from TCAD Silvaco.

Figure 5 shows the curve between the g_m/I_d ratio based on the drain bias for DH-DD-TM-SG MOSFETs for various values of channel length. There is smaller value of g_m/I_d at higher values of drain bias. This is mainly due to the punch through as a result of large electric field near the drain. It is observed from the figure that as the value of channel length increases, the g_m/I_d value also increases. So DH-DD-TM-CGAA MOSFETs will be more beneficial for analog circuit applications. The analytical results are well correlated with the simulation results proving the accuracy of proposed model.

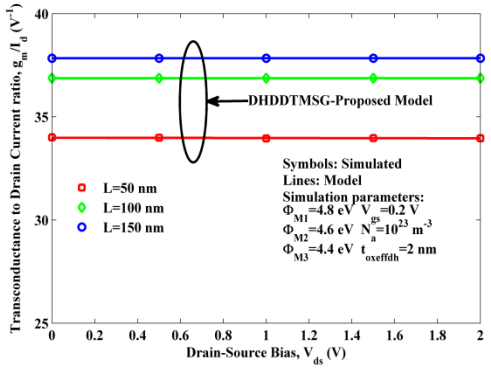

Figure 5. TDCR as a function of the drain source bias at different channel length for DH-DD-TM-CGAA MOSFET

4. COMPARISION of DH-DD-TM-SG and TM-SG

The TDCR of DH-DD-TM-SG MOSFET is estimated for different lengths along the channel. Figure 6 shows the TDCR of proposed device and TM-SG with channel length. The triple metal/material surrounding gate MOSFET is used for making comparative analysis with the proposed model. Since the TM-SG MOSFET uses similar approach to find out the TDCR, so it is used for comparison. As obvious from Figure 6 as well as from the Table 1 that DH-DD-TM-CGAA MOSFET provides higher value of TDCR than the TM-SG MOSFET. The g_m/I_d ratio will be increased whenever there will be an incremental change in the channel length. Moreover it is clearly visible from the figure that due to the presence of SCEs [19], there is significant reduction in the g_m/I_d ratio at lower channel lengths. Hence the DH-DD-TM-CGAA MOSFETs can be used in micro power circuit applications where higher TDCR is essential.

Figure 7 shows the dependence of g_m/I_d ratio on varying silicon film thickness at an appropriate channel length for DH-DD-TM-CGAA and TM-SG MOSFETs. As evident from Figure 7 and Table 2, it can be concluded that the DH-DD-TM-SG MOSFET shows a peak g_m/I_d ratio $34V^{-1}$whereas TM-SG attain $33.1V^{-1}$ at t_{si}=20nm. The ratio decreases with respect to increase in silicon film thickness. The simulated results are compared with analytical results and close agreement is obtained.

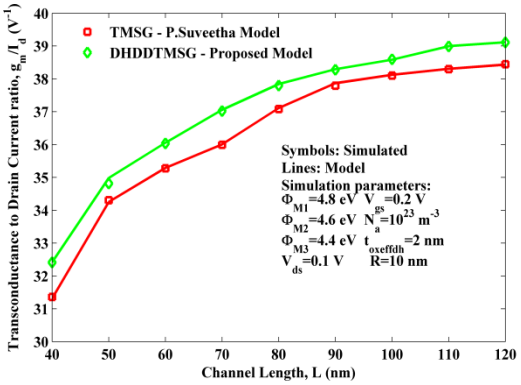

Figure 6. TDCR of TMDDCGAA and DH-DD-TM-CGAA MOSFET at various channel length

TABLE 1. G_m/I_d values at different channel length

L (nm)	G_m/I_d (V^{-1})	
	TM-SG	DH-DD-TM-SG
40	31.35	32.41
60	35.27	36.03
80	37.08	37.79
100	38.09	38.59
120	38.44	39.01

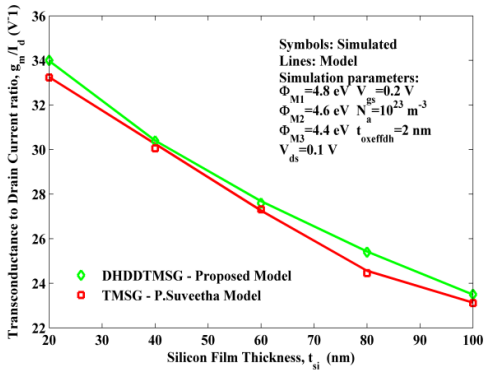

Figure 7. TDCR on varying silicon film thickness for DH-DD-TM-CGAA and TM-SG MOSFET

TABLE 2. G_m/I_d values for different Silicon thickness

T_{si} (nm)	G_m/I_d (V^{-1})	
	TM-SG	DH-DD-TM-SG
20	33.13	34.00
40	30.05	30.38
60	27.31	27.59
80	24.45	25.37
100	23.10	23.50

5. CONCLUSIONS

In this paper, an accurate 2-D analytical model for g_m/I_d ratio of the novel device DH-DD-TM-SG MOSFET has been presented and scrutinized. The small signal MOSFET model, which is mandatory to determine the frequency behavior, is beyond the scope of present analysis. The study was then continued to obtain higher g_m/I_d values for all combination of device parameters. Further, the TDCR model of proposed device has been compared with the TM-SG strucure. The g_m/I_d value of DH-DD-TM-SG MOSFETs does not fall down at smaller channel lengths and larger silicon film thickness unlike that of TM-SG MOSFETS. The higher g_m/I_d ratio of DH-DD-TM-SG MOSFETs is beneficial for designing of analog circuits. Therefore it is concluded that the g_m/I_d ratio could be intensified by integrating the dual halo with dual dielectric instead of TM-SG MOSFETs design.

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چکیده

یک مدل MOSFET با یک دیود الکترومغناطیسی سه گانه (DH-dual-hialo-gate-all-around / gateway DD-TM-CGAA / SG) پیشنهاد شده است و یک مدل تحلیلی برای نسبت جریان فعلی به تخلیه (TDCR) توسعه داده شده است. ترکیب دوگانه با مواد دو الکتریکی و سه بعدی موجب افزایش عملکرد دستگاه از لحاظ بهبود TDCR می شود. در اثر TDCR برای تغییرات در پارامترهای دستگاه مانند ضخامت اکسید، ضخامت سیلیکون، غلظت doping کانال، طول کانال و تخریب تخلیه تجزیه و تحلیل شده است. نتایج نشان می دهد که مقدار بزرگتر از g_m/I_d در دستگاه پیشنهادی در مقایسه با سایر سه گانه موجود ساختارهای مادی است که آن را برای برنامه های کاربردی میکرودرمی مناسب می سازد. نتایج تحلیلی مدل g_m/I_d توسعه یافته به شدت با نتایج شبیه سازی شده از TCAD Silvaco موافق است.

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