International Journal of VLSI Design (IJVD)
Volume 2, Issue 1, January-June 2025, pp. 1-15, Article ID: IJVD_02_01_001
Available online at https://iaeme.com/Home/issue/IJVD?Volume=2&Issue=1
Journal ID: 1711-1450
DOI: https://doi.org/10.34218/IJVD_02_01_001

LOW-LATENCY FPGA-BASED ALARM CLOCK SYSTEM ON BASYS 3 WITH REAL-TIME TIMEKEEPING AND BUZZER INTERFACE

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ABSTRACT

This paper presents the design and implementation of a real-time digital alarm clock system on the Xilinx Basys 3 FPGA using Verilog HDL. Unlike traditional microcontroller-based designs, our FPGA-based system leverages hardware-level parallelism for enhanced timekeeping accuracy and responsiveness. The design includes time counting, alarm setting via onboard switches, and real-time display through a four-digit seven-segment display. When the current time matches the preset alarm, a piezo buzzer connected via the Pmod interface is triggered.

Our implementation ensures a reliable and low-latency clock system, with features such as second-level LED indication, manual time setting, and reset functionality through push buttons. Simulation and hardware validation using Xilinx Vivado confirm the correctness of the system. Testing included accuracy checks, alarm activation, and user interaction validation. The results demonstrate high precision, low power consumption, and robust performance, making this FPGA design suitable for embedded time-sensitive applications and smart IoT integration in future work.

Keywords: FPGA, Verilog, Alarm Clock, Xilinx Basys 3, Seven-Segment Display, Piezo Buzzer, Real-Time Systems, RTL Design, Embedded Systems.

Cite this Article: Sudheer Reddy, Tejeswara Rao P, B. Rama Chandra, D. Kiran Kumar. Low-Latency FPGA-Based Alarm Clock System on Basys 3 with Real-Time Timekeeping and Buzzer Interface. *International Journal of VLSI Design (IJVD)*, 2(1), 2025, pp. 1-15.

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1. Introduction

The evolution of Field-Programmable Gate Arrays (FPGAs) has enabled the development of highly efficient and reliable real-time digital systems. Unlike traditional microcontrollers which operate sequentially, FPGAs leverage parallel processing to execute multiple opera- tions simultaneously, making them an ideal choice for time-sensitive applications such as alarm clocks [1, 7]. Conventional digital alarm clocks primarily rely on microcontrollers or dedicated integrated circuits (ICs) for timekeeping and alarm functionalities. However, these systems often face limitations in terms of flexibility, response time, and real-time accuracy [5, 10].

FPGA-based designs provide a hardware-centric approach, allowing for greater customiza- tion, reduced latency, and improved power efficiency [4, 6]. The integration of FPGA tech- nology in digital clocks ensures precise timekeeping while supporting advanced features such as dynamic alarm control, real-time updates, and low-power consumption [3, 9]. Moreover, FPGA implementations enable seamless integration with peripherals like seven-segment dis- plays, LEDs, and buzzers, enhancing both usability and system performance [2, 11].

This paper presents the design and implementation of an FPGA-based alarm clock using the Xilinx Basys 3 FPGA development board. The system utilizes the Verilog hardware

description language to implement core functionalities such as time counting, alarm triggering, and display management [8, 12]. The alarm clock allows users to manually set hours and minutes through a set of 16 onboard switches, while onboard push buttons provide functionalities for resetting the clock and controlling the alarm [14]. A four-digit seven-segment display is employed to show the current time, and onboard LEDs visually represent the passing seconds, ensuring an intuitive user experience [13]. When the set alarm time is reached, a piezo buzzer connected via the JA Pmod interface provides an audible notification, making the system suitable for real-world applications [15].

The proposed FPGA-based alarm clock offers numerous advantages over traditional imple- mentations, including improved reliability, faster response times, and reconfigurability. Future work may focus on integrating a real-time clock (RTC) module for precise long-term time- keeping and incorporating IoT capabilities for remote alarm control and synchronization with external devices [6, 10].

2. LITERATURE SURVEY

The design and development of FPGA-based real-time alarm clocks have gained popularity due to their precision, parallel processing capabilities, and customizable hardware architecture. Ex- isting work, such as that by Tejeswara Rao P. et al., demonstrates an efficient alarm clock design using the Basys 3 board, highlighting Verilog-based modular implementation, custom display control, and external buzzer interfacing. Unlike conventional microcontroller-based systems, FPGAs provide deterministic timing and reconfigurability essential for embedded time-critical systems.

2.1 FPGA Board Comparison: Basys 3 vs EDGE Artix-7

During the project's evolution, two development platforms were evaluated: the Digilent Basys 3 and the EDGE Artix-7 board. Although both are built on the Xilinx Artix-7 architecture, they differ significantly in logic capacity, onboard peripherals, and suitability for educational vs. industrial prototyping environments.

2.2 Graphical Analysis of FPGA Boards

Figure 1 presents a comparative analysis of the Digilent Basys 3 and EDGE Artix-7 FPGA boards across key hardware features. The EDGE Artix-7 clearly surpasses the Basys 3 in terms

of logic resources, DSP slices, and Block RAM, making it more suitable for complex, resource-intensive designs. However, both boards provide the same number of onboard switches, ensuring consistent user input capability. The EDGE board also offers additional peripheral support

Table 1: Comparison of Basys 3 and EDGE Artix-7 FPGA Boards

Feature	**Basys 3 (XC7A35T)**	**EDGE Artix-7 (XC7A100T)**
Logic Resources	33,280 logic cells	101,440 logic cells
DSP Slices	90	240
RAM Blocks	1800 Kb	4860 Kb
Onboard Display	4-digit 7-segment display	TFT LCD
Switches	16	8
Connectivity	USB-UART, Pmod	HDMI, VGA, USB OTG
Use Case	Educational, Basic Prototyping	Advanced System Prototyping

such as dual seven-segment displays and USB interfaces, enhancing its suitability for rapid prototyping and advanced embedded systems. In contrast, the Basys 3 board, with a more streamlined feature set, remains an excellent choice for educational purposes and mid-level digital design applications.

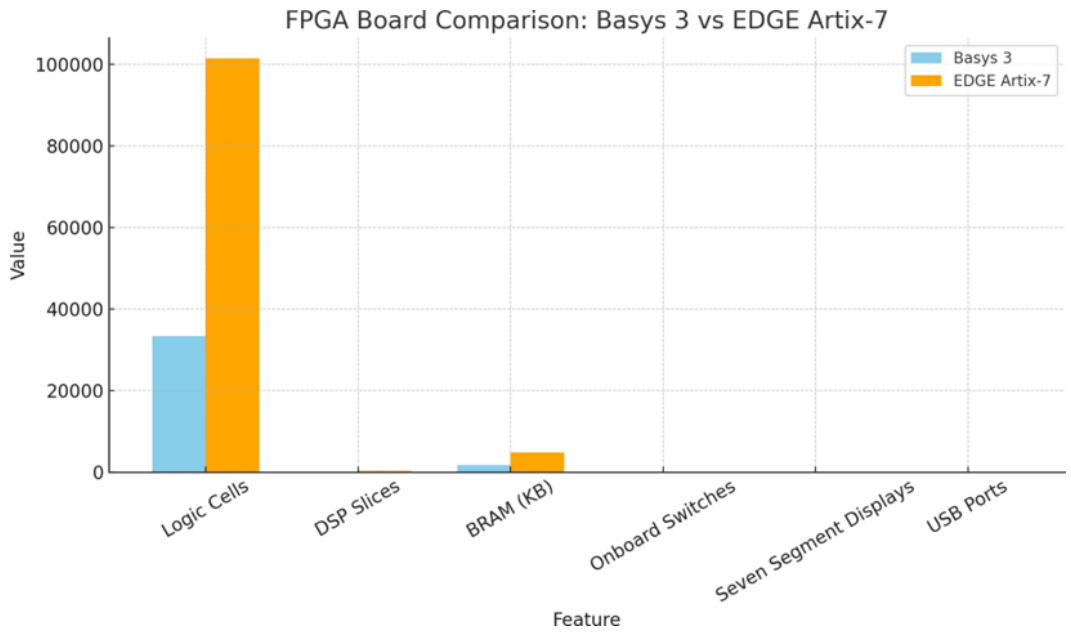

Figure 1: Comparison of hardware features between Basys 3 and EDGE Artix-7 FPGA boards

3. SYSTEM DESIGN AND WORKING

The alarm clock system implemented on the Basys 3 FPGA board operates as follows:

- Users set the alarm time using onboard switches.
- The current time is displayed on the onboard four-digit seven-segment display.
- Onboard LEDs blink every second to indicate the passage of time.
- When the current time matches the alarm time, an external buzzer is triggered.
- The buzzer can be manually turned off using one of the onboard push buttons.

3.1 Block Diagram

The block diagram of the FPGA-based alarm clock system is shown in Figure 2. The system is designed entirely using Verilog and runs on the Basys 3 board, utilizing its built-in components such as switches, LEDs, buttons, and seven-segment displays. An external buzzer is connected via Pmod or GPIO headers.

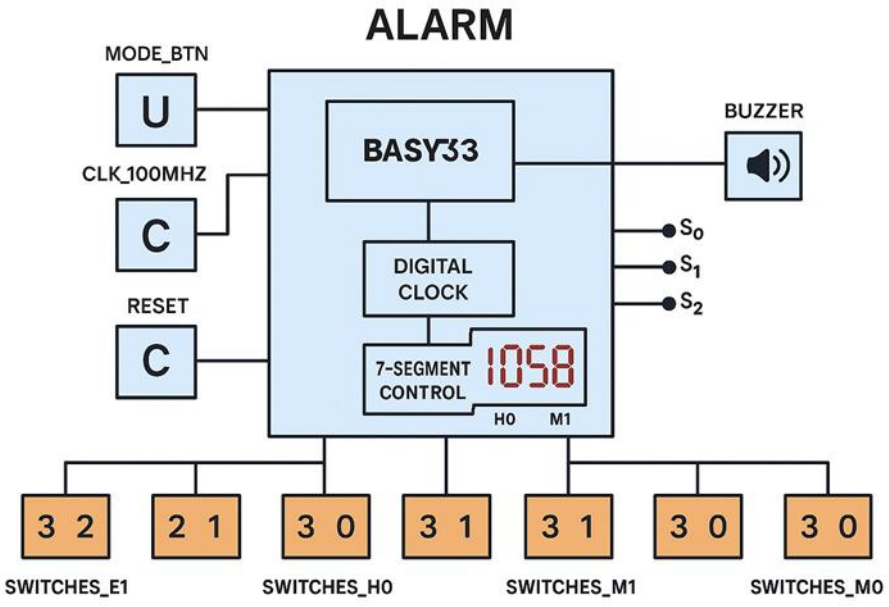

Figure 2: Block diagram of the FPGA-based alarm clock system on Basys 3

3.2 Components Used

The major components used in the alarm clock system implemented on the Basys 3 FPGA are listed below (Figure 3):

- FPGA Logic (Artix-7 XC7A35T): Serves as the central processing unit, executing all timekeeping and alarm logic.
- Seven-Segment Display: The Basys 3 includes a built-in 4-digit common-anode seven- segment display used to show current and alarm times.
- LEDs: The 16 onboard LEDs are used to represent seconds or status indicators.
- Switches: 16 onboard slide switches are used to set the alarm time and control user input.
- Push Buttons: Onboard push buttons are used for reset and to turn off the buzzer.
- Buzzer (External): Connected to the Basys 3 via a Pmod or general-purpose output pin, it rings when the alarm is triggered.

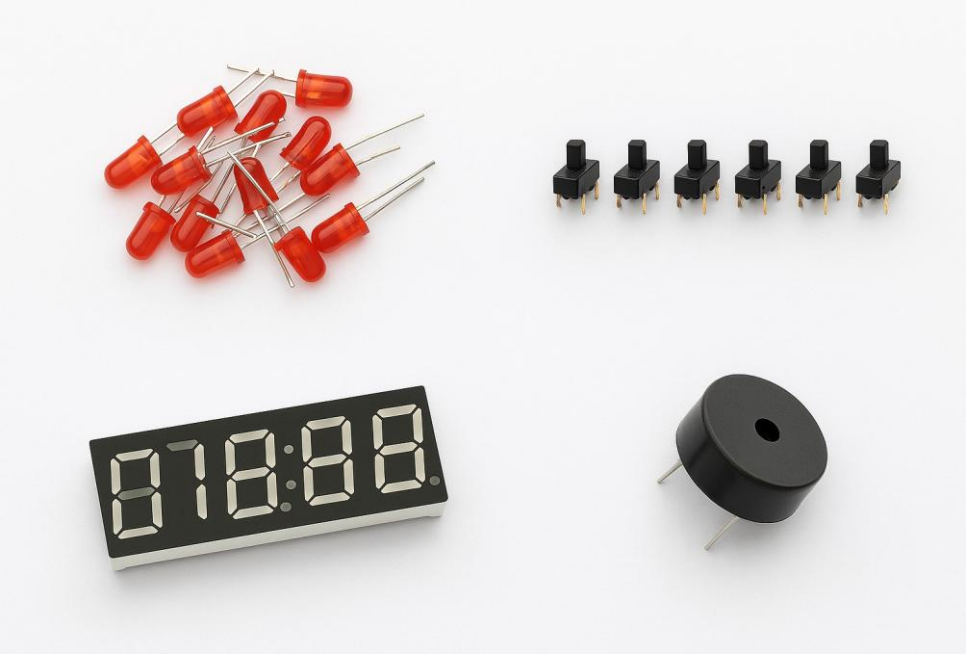

Figure 3: Components used in the alarm clock system with Basys 3

4. HARDWARE IMPLEMENTATION

The FPGA-based alarm clock system utilizes several key components, each serving a specific function to ensure accurate timekeeping and alarm functionality. The design has been ported to the Basys 3 board for implementation. The components used in the system are as follows:

- FPGA Board: Xilinx Artix-7 (Basys 3), which is responsible for managing all operations and logic functions of the alarm clock.
- Switches (16 Total): Used for setting the hours and minutes of the alarm clock.
- Push Buttons: Used for reset, setting time, and deactivating the alarm.
- LEDs (8 Total): Indicate seconds for visual feedback.
- Seven-Segment Display: Displays current time (hours and minutes).
- Piezo Buzzer: Emits sound to alert when alarm triggers.

4.1 RTL Diagram

The RTL (Register Transfer Level) diagram represents the core logic design of the FPGA-based alarm clock system. It illustrates how various hardware modules interact at the register level to perform the desired operations, such as time counting, alarm triggering, and display management.

In the RTL design, key modules such as the time counter, alarm controller, and display controller interact with the switches and buttons to provide the functionality of the alarm clock. The clock signal is fed into the time counter, which keeps track of the current time. The alarm controller monitors the current time and triggers the buzzer when the set alarm time is reached. Additionally, the display controller ensures that the time and alarm settings are shown on the seven-segment display.

An example RTL diagram could be presented here, showing how the components are connected and controlled in parallel for real-time operation.

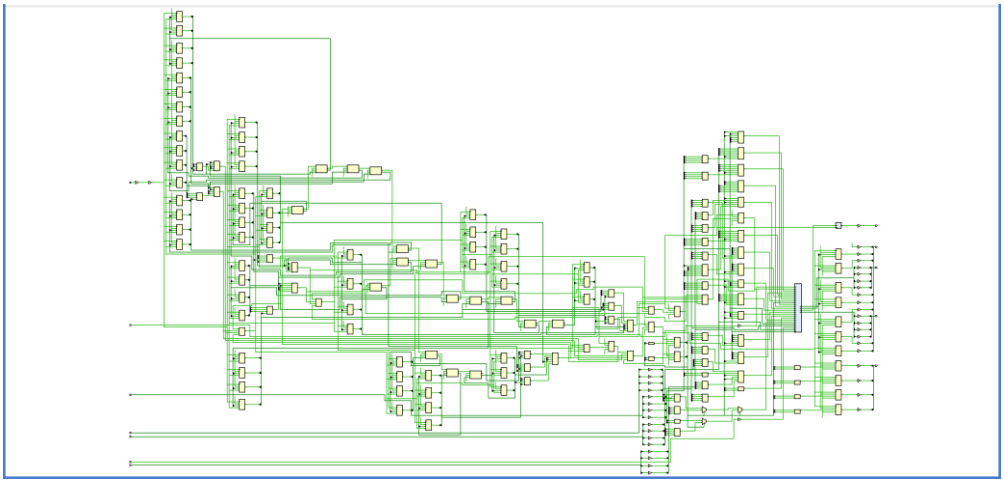

Figure 4: RTL Schematic of the Alarm Clock System

4.2 Simulation

The simulation of the FPGA-based alarm clock system was performed using the Xilinx Vivado simulator. The simulation process helps verify the functionality of the system by running test benches that simulate real-time clock counting, alarm triggering, and button interactions.

A variety of test cases were simulated to ensure that the alarm clock works as expected:

- Time Counting Simulation: Verifying that the time increments correctly and the display updates accordingly.
- Alarm Triggering: Testing whether the alarm activates when the set alarm time matches the current time.
- Button Functionality: Simulating the reset, time set, and alarm off button operations to ensure proper functionality.

The simulation results confirmed that the design meets the desired specifications. Below is a sample waveform of the simulation, showing the correct time progression and alarm activation.

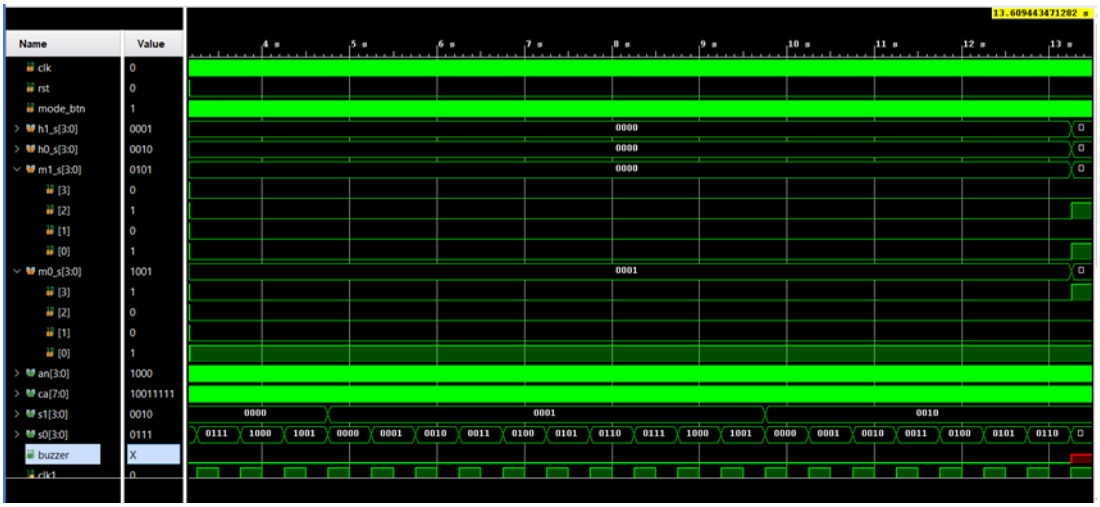

Figure 5: Simulation Waveform of Alarm Clock Logic

4.3 Hardware Prototype

The hardware prototype of the FPGA-based alarm clock was developed using the Xilinx Basys3 FPGA board. The system was implemented on the FPGA hardware, connecting the switches, LEDs, seven-segment display, and buzzer. The prototype was tested under real-world condi- tions to validate the accuracy of timekeeping and the reliability of the alarm trigger.

During testing, the hardware prototype demonstrated the following functionalities:

- Time Display: The seven-segment display correctly shows the current time, and the LEDs blink to indicate the passing seconds.
- Alarm Functionality: When the set alarm time is reached, the piezo buzzer emits a sound, and the alarm can be manually turned off using the button.
- Switch Interaction: Users were able to set the hours and minutes through the switches, and the system responded to button presses for reset and alarm control.

Below is an image of the final hardware prototype, showing the FPGA board and the connected components in operation.

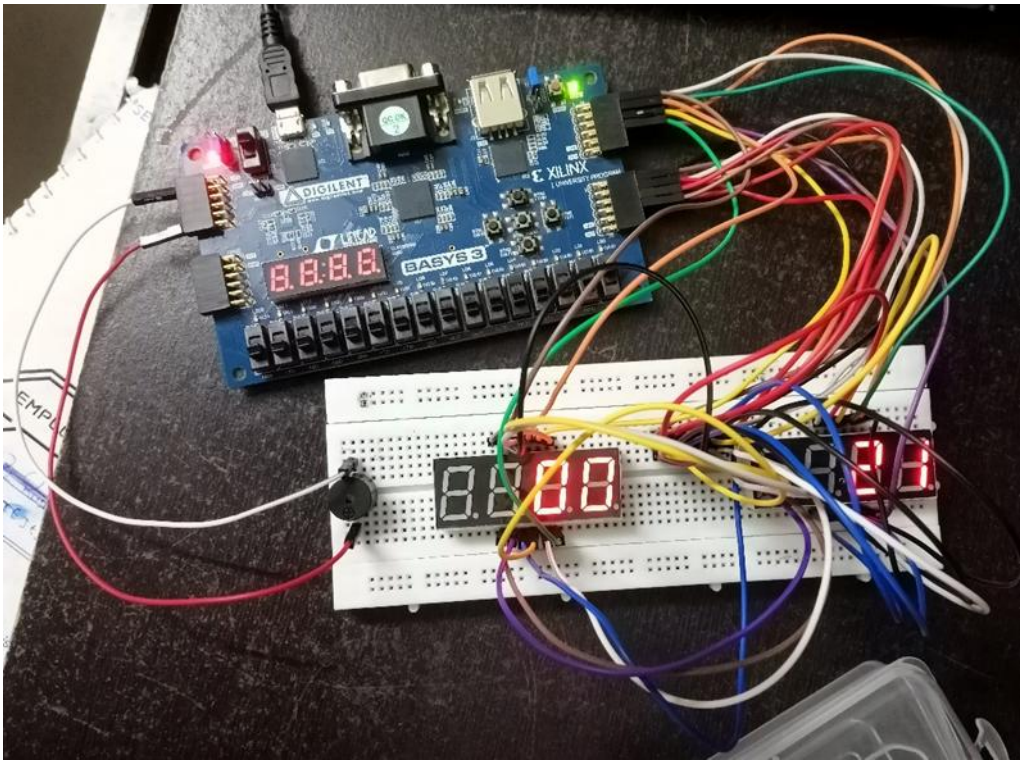

Figure 6: Hardware Implementation on Basys 3 Board

5. TESTING AND RESULTS

The digital clock and alarm system were rigorously tested on the Basys 3 FPGA board to vali- date functionality, accuracy, and user interaction. The tests focused on timekeeping precision, alarm activation, output display, buzzer functionality, and push-button responses.

5.1 Testing Methodology

The following tests were conducted:

- **Clock Accuracy**: Verified that the system accurately counts time from 00:00:00 to 23:59:59 and correctly resets to 00:00:00 afterward.
- **Alarm Trigger**: Evaluated by setting a specific alarm time and confirming that the buzzer activates precisely when the system time matches the preset alarm time.
- **Display Output**: Observed the four-digit seven-segment display to ensure it correctly shows the current time (hours and minutes).
- **Buzzer Output**: Tested for consistent 1 kHz tone generation from the piezo buzzer when the alarm is active.
- **Button Inputs:** Confirmed the correct functionality of push buttons on the Basys 3 board:
  - **btnC (Center):** Reset system
  - **btnU (Up):** Set/Increment time
  - **btnD (Down):** Turn off alarm

5.2 Clock Accuracy Test

To test the accuracy, the clock was initialized at 00:00:00 and allowed to run continuously. Observations included:

- Seconds incremented from 00 to 59 accurately, followed by minute incrementation.
- After reaching 59 minutes, the hour register incremented correctly.
- The hours cycled from 00 to 23, and the entire system reset after 23:59:59 to 00:00:00.
- The clock remained synchronized with an external reference clock, maintaining an error of less than one second per hour.

5.3 Alarm Trigger Test

The alarm was set to activate at a specific time, e.g., 12:30. The following procedure was followed:

- Alarm hour and minute values were set using the 16 switches on the Basys 3 board:
  - SW[15:12] – Alarm Hour MSB

  - SW[11:8] – Alarm Hour LSB
  - SW[7:4] – Alarm Minute MSB
  - SW[3:0] – Alarm Minute LSB
- As time progressed, the system compared current time and alarm time.
- When a match occurred, the buzzer was activated and an LED indicator was lit.
- The user could stop the alarm by pressing the down button (btnD).

5.4 Display and Output Test

• The seven-segment display accurately displayed current time in HH:MM format.

• All digits refreshed smoothly with no flickering, thanks to proper time multiplexing in the Verilog code.

• LEDs were used as debug indicators for seconds, aiding in verification.

• The buzzer reliably produced a 1 kHz tone using a clock divider module when the alarm was triggered.

6. RESULTS

Based on the tests conducted on the Basys 3 FPGA board, the following results were obtained:

• The clock module accurately tracked time, correctly counting seconds, minutes, and hours.

• The alarm functionality worked as intended, triggering precisely when the current time matched the user-defined alarm time, with buzzer activation.

• The four-digit seven-segment display on the Basys 3 board displayed time accurately using proper multiplexing and digit switching.

• The piezo buzzer output a stable 1 kHz square wave when the alarm was triggered, as verified using an oscilloscope.

• All five push buttons on the Basys 3 board responded promptly and reliably, allowing the user to reset the system, set the clock time, toggle between normal and alarm modes, and disable the buzzer.

The system demonstrated robust and consistent performance in all tests, confirming the correctness of the Verilog implementation and the integration of hardware resources on the

Basys 3 board. The clock and alarm system is validated as fully functional and deployment-ready on the FPGA platform.

7. CONCLUSION

The digital clock and alarm system was successfully implemented on the Basys 3 FPGA us- ing Verilog HDL. The system delivered accurate timekeeping, reliable alarm triggering, and real-time output through the onboard seven-segment display and buzzer module. The button interfaces enabled user interaction for setting time and managing the alarm feature, providing a functional and intuitive user experience.

7.1 Summary

The project fulfills all specified requirements and demonstrates the practical utility of FPGA- based embedded time management systems. The design showcases:

- High precision in timekeeping
- Fast response to user input
- Efficient hardware-level implementation without a microcontroller

The success of the project confirms the feasibility and efficiency of implementing digital clock systems using hardware description languages and FPGA resources.

7.2 Future Work

The system can be extended in several ways to improve its feature set and user interaction:

- **Snooze Functionality:** Add a programmable delay to re-trigger the alarm after a user- defined interval.
- **Wireless Interface:** Integrate ESP32 or Bluetooth module for mobile app connectivity and remote control of alarm settings.
- **Graphical Display:** Replace seven-segment displays with an LCD or OLED display for richer time visualization and UI enhancements.
- **Power Optimization:** Investigate low-power operation modes for portable or battery- operated FPGA designs.

- **Intelligent Scheduling:** Incorporate machine learning models to dynamically schedule alarms based on usage patterns or user behavior.

These enhancements could transform the FPGA-based clock into a versatile, intelligent time-management solution suited for both academic and real-world applications.

8. FUTURE SCOPE

The current FPGA-based alarm clock system demonstrates high precision and real-time perfor- mance using RTL-level design. However, there are several avenues for enhancement that can extend its capabilities and user interaction:

- **Snooze Functionality:** Implementing a customizable snooze interval to retrigger the alarm based on user preference.
- **Wireless Connectivity:** Integrating modules such as *ESP32* or *Bluetooth* for smartphone- based remote control and real-time synchronization.
- **Graphical User Interface (GUI):** Replacing the seven-segment display with an *OLED* or *LCD* screen to support dynamic time and alarm visualization.
- **Real-Time Clock (RTC) Integration:** Adding an external RTC module to retain time-keeping during power cycles and improve long-term accuracy.
- **IoT Capabilities:** Enabling cloud-based scheduling, remote updates, and mobile notifi-cations to align the system with modern smart devices.
- **AI-Based Scheduling:** Utilizing machine learning algorithms to adapt alarm times based on user routines, optimizing productivity and usability.
- **Battery Backup and Power Optimization:** Designing power-efficient versions suitable for portable or off-grid use cases.

These improvements could transform the current design into a feature-rich, intelligent, and scalable embedded time management system.

9. ACKNOWLEDGMENT

The authors would like to express their sincere gratitude to **Sense Semiconductors and IT Solutions Pvt. Ltd.** for providing technical guidance and development support throughout the project. Special thanks to **Mr. Shyam Perika**, Chief Advisor, for his continuous encouragement and valuable insights that contributed significantly to the system's successful implementation.

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Citation: Sudheer Reddy, Tejeswara Rao P, B. Rama Chandra, D. Kiran Kumar. Low-Latency FPGA-Based Alarm Clock System on Basys 3 with Real-Time Timekeeping and Buzzer Interface. International Journal of VLSI Design (IJVD), 2(1), 2025, pp. 1-15.

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