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## **A Knowledge Graph-Based AI Framework for Managing Functional Validation Complexity in Next-Generation SoC Platforms**

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### **Abstract**

The increasing complexity of next-generation System-on-Chip (SoC) platforms poses significant challenges in functional validation. Traditional approaches struggle with managing the expanding validation coverage, data volume, and integration scenarios. This paper proposes a novel AI-driven framework leveraging knowledge graphs (KGs) to systematically manage validation complexity by organizing heterogeneous validation data, capturing interdependencies, and enabling intelligent automation in test planning and bug localization. Our experiments show that integrating KGs can improve validation efficiency by 35% compared to conventional methods. The results demonstrate that this approach enhances traceability, boosts decision-making, and reduces the overall effort required in functional validation.

**Keywords:** Knowledge Graphs, Artificial Intelligence, Functional Validation, System-on-Chip (SoC), Verification Automation, Bug Localization

### **1. Introduction**

The surge in functionality, heterogeneity, and integration density in modern SoCs demands sophisticated validation techniques. Traditional functional validation approaches, primarily based on manual planning and random coverage models, are no longer sufficient. The volume of data generated during simulation, emulation, and prototyping phases can overwhelm even expert teams, leading to gaps in coverage and delayed time-to-market. Recent advances in AI and graph-based data representations offer a compelling opportunity to rethink validation workflows.

Knowledge graphs, widely successful in domains like web search and bioinformatics, can model complex, evolving relationships among validation artifacts. Applying KGs to SoC validation can streamline bug tracing, prioritize test execution, and recommend coverage strategies. However, the application of KGs in semiconductor validation remains largely underexplored. This paper presents an AI framework using knowledge graphs to manage functional validation complexity, automating critical tasks and enhancing engineering productivity.

## **2. Problem Statement**

The functional validation of next-generation System-on-Chip (SoC) platforms is becoming increasingly complex due to the growing integration of heterogeneous components, aggressive time-to-market pressures, and the explosive expansion of validation data. Traditional validation approaches, which rely heavily on manual processes, constrained-random testing, and coverage metrics, are struggling to scale with the evolving demands.

Manual management of validation artifacts often leads to incomplete coverage, missed corner cases, and delayed bug discovery. Additionally, regression analysis across multiple revisions becomes extremely cumbersome, resulting in redundant test executions and inefficient resource utilization. Root cause analysis (RCA) remains a bottleneck, often requiring significant manual effort to trace failure paths in large validation datasets. Context-aware test generation, which could potentially prioritize critical validation scenarios, is rarely automated, leading to a proliferation of irrelevant or redundant test cases. These bottlenecks collectively inflate validation cost, delay project timelines, and increase the risk of post-silicon bugs escaping into production.

There is a compelling need for a scalable, intelligent validation management system that can systematically organize validation data, automate dependency tracking, and optimize validation activities. A knowledge graph-based AI framework promises to address these challenges by enabling semantic modeling of validation artifacts, intelligent test planning, faster bug localization, and dynamic adaptation to validation progress. However, no comprehensive solutions currently exist that integrate knowledge graphs with AI-driven reasoning specifically tailored to SoC functional validation complexity.

## **3. Literature Review**

### **3.1 Overview**

The rapid evolution of SoC (System-on-Chip) platforms has intensified the complexity of functional validation. Existing validation approaches increasingly struggle with scalability, traceability, and automation. The following review discusses major contributions to functional validation, graph-based representations, machine learning applications in SoC verification, and identifies critical gaps addressed by our proposed framework.

### 3.2 Functional Validation Techniques

Functional validation traditionally relies on coverage-driven verification (CDV) and constrained-random test generation. Mishra and Li (2018) emphasized graph-based models for microarchitecture validation to track test coverage more systematically. However, their work was limited to core-level validation, without addressing SoC-level complexity. Ferguson et al. (2018) proposed graph databases for managing verification data but did not integrate semantic knowledge or AI-driven optimization.

### 3.3 Machine Learning for Validation

Machine learning techniques have been increasingly explored for functional debug and bug localization. Kapoor and Zhao (2019) introduced clustering methods to accelerate debug cycles in validation. Similarly, Gupta et al. (2019) proposed ML techniques for post-silicon validation to predict bug-prone regions. While these approaches improved specific aspects of validation, they lacked a comprehensive structure for organizing validation knowledge systematically.

### 3.4 Knowledge Graph Applications

Knowledge graphs (KGs) have demonstrated success in modeling complex relationships across various domains. Zandifar et al. (2020) applied KGs in the domain of design rule validation, offering insights into cross-domain dependencies. However, KG applications specific to functional validation have been rare. Yoon et al. (2017) explored knowledge discovery in validation but without a structured KG approach.

### 3.5 AI in SoC Validation

Recent efforts such as Chen and Wang (2020) showcased predictive validation using AI for mobile SoCs. They demonstrated that machine learning could predict test outcomes based on historical execution patterns. Similarly, Patel et al. (2020) explored deep learning techniques for validation failure prediction. Yet, these methods focus mainly on predictive modeling and overlook knowledge-driven validation process management.

### 3.6 Identified Gaps

A significant gap exists in leveraging **knowledge graph-based AI frameworks** to unify functional validation data, automate test planning, and enhance bug localization. Most existing solutions are domain-specific, heuristic-driven, or lack semantic richness. Our work proposes a comprehensive KG framework that not only models validation artifacts but also applies AI reasoning to optimize validation workflows end-to-end.

## 4. Proposed Framework

The proposed Knowledge Graph (KG)-based AI framework for managing functional validation complexity in SoC platforms is structured into six interconnected layers. Each layer plays a vital role in organizing validation artifacts, enabling intelligent reasoning, and automating key validation tasks.

The layers of the framework are:

#### **4.1 Artifact Ingestion**

This layer collects diverse validation artifacts, including simulation outputs, test specifications, coverage data, emulation logs, and bug reports. Both structured and unstructured data are processed through parsing engines and ingestion pipelines. Important metadata such as timestamps, testbench configurations, and simulation conditions are captured to ensure traceability.

#### **4.2 Semantic Annotation**

The ingested artifacts are enriched with semantic labels using Natural Language Processing (NLP) and rule-based heuristics. Validation artifacts are classified into ontological categories such as "TestCase", "FailureMode", "CoverageGoal", and "BugReport". Semantic relationships, such as "tests covers feature" or "bug impacts module", are established to prepare the data for graph construction.

#### **4.3 Knowledge Graph Construction**

The semantically annotated artifacts are then mapped into a graph structure where nodes represent entities (e.g., tests, coverage points, design blocks) and edges represent relationships (e.g., "verifies", "fails", "blocks"). This graph evolves dynamically as new validation artifacts are added, providing a living model of the validation ecosystem.

#### **4.4 Validation Intent Modeling**

AI techniques such as classification and clustering are applied to model validation intents. This includes predicting which tests are likely to impact which design features and identifying missing coverage areas. Embedding-based methods like GraphSAGE are utilized to learn representations of graph nodes, supporting intent similarity analysis.

#### **4.5 Test Planning Optimization**

Based on the learned graph model, the framework generates optimized test execution plans. Tests are prioritized according to their expected coverage contribution and relevance to recent design changes. Redundant tests are minimized, and previously low-yield tests are flagged for retirement or restructuring.

#### **4.6 Bug Localization and Root Cause Analysis**

When a validation failure occurs, the KG is traversed to identify the most probable bug locations based on impact propagation paths and historical failure patterns. AI reasoning further enhances RCA (Root Cause Analysis) by correlating new bugs with previously known failure modes embedded in the knowledge graph.

### **5. Experimental Results and Discussion**

To evaluate the effectiveness of the proposed knowledge graph (KG)-based AI framework for functional validation, we conducted experiments on a real-world mobile SoC validation project. The

experimental dataset consisted of approximately 50,000 artifacts, including test specifications, coverage reports, simulation logs, and bug reports, collected across three product validation cycles.

The key performance metrics analyzed were **Bug Triage Time Reduction (BTR)**, **Coverage Closure Acceleration (CCA)**, and **Test Redundancy Reduction (TRR)**. To quantify improvements, we define a normalized improvement function  $I_m$  for each metric  $m$  as:

$$I_m = \frac{V_{\text{baseline}} - V_{\text{KG}}}{V_{\text{baseline}}} \times 100\%$$

where:

- $V_{\text{baseline}}$  = Performance metric using traditional validation method,
- $V_{\text{KG}}$  = Performance metric using the KG-based AI framework.

## Results Summary

Applying this equation to our experimental data, we observed:

- **Bug Triage Time Reduction (BTR)** = 35%
- **Coverage Closure Acceleration (CCA)** = 25%
- **Test Redundancy Reduction (TRR)** = 40%

These results show significant validation efficiency gains when using the KG-based framework compared to traditional methods.

Metric	Baseline Method (%)	KG-based Framework (%)	Improvement (%)
Bug Triage Time	100	65	35
Coverage Closure Time	100	75	25
Redundant Tests Executed	100	60	40

## 6. Discussion:

The experiment demonstrated that knowledge graphs effectively structured validation knowledge, significantly reducing search space during bug localization and coverage analysis. By semantically linking validation artifacts, tests impacted by specification changes were automatically identified, preventing redundant execution. Moreover, AI-driven intent modeling of validation targets prioritized under-verified functionalities, accelerating coverage closure. These results validate the

framework's ability to manage validation complexity systematically and improve resource efficiency.

Furthermore, the framework exhibited adaptability across multiple SoC validation cycles, showing that knowledge evolution in the graph can dynamically refine validation strategies over time. This suggests that future applications could integrate post-silicon feedback into the knowledge graph to continually optimize validation flows.

## 7. Conclusion and Future Work

This paper demonstrated that knowledge graphs, combined with AI reasoning, offer a powerful mechanism to manage functional validation complexity in next-generation SoCs. The framework can be extended with federated KGs to integrate external test specifications or third-party IP validation results. Future work includes dynamic graph evolution to accommodate post-silicon learning and continuous validation adaptation.

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