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Formal Verification of Safety-Critical Control Flow in Distributed Embedded Systems Using Model Checking and Symbolic Executions

Chloe Thompson,
Canada.

Abstract

Ensuring the correctness of control flow in distributed embedded systems is vital, particularly in safety-critical domains like automotive, aerospace, and industrial automation. Traditional testing is often insufficient due to the system's distributed nature and real-time constraints. This paper proposes a hybrid approach that combines model checking and symbolic execution to verify the safety properties of distributed control flows. We analyze control flow correctness, deadlock-freedom, and reachability through formal methods applied to a representative system architecture. Our findings demonstrate that the integrated approach can reveal latent faults undetected by conventional testing and simulation-based techniques. Experimental results validate the efficacy of this method in detecting critical errors with acceptable computational overhead.

Keywords: Formal verification, Model checking, Symbolic execution, Distributed embedded systems, Control flow analysis, Safety-critical systems, Real-time systems, Deadlock detection.

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1. Introductıon

Distributed embedded systems (DES) have become ubiquitous in modern safety-critical environments, including avionics, automotive systems, and medical devices. These systems are characterized by concurrency, real-time constraints, and strict correctness requirements. The complexity of such systems introduces significant risks, especially when control flow errors propagate undetected across nodes. As such, ensuring safe control flow through rigorous verification is indispensable.

Formal methods offer a principled solution by allowing mathematical reasoning about system properties. However, applying them in real-world DES remains challenging due to scalability, abstraction, and non-determinism. This paper explores a combined strategy using model checking and symbolic execution to overcome these limitations. Model checking provides exhaustive state-space exploration, while symbolic execution complements it by efficiently analyzing input-dependent execution paths.

2. Literature Review

Formal verification of embedded systems has gained substantial traction, particularly with model checking tools like SPIN and NuSMV. Clarke et al. (2012) emphasized the feasibility of model checking in verifying finite-state distributed systems. However, scalability remains an issue in industrial-scale applications.

Symbolic execution has evolved as a complementary approach. Godefroid et al. (2011) introduced *KLEE*, which effectively analyzed complex execution paths in C programs. Similarly, Anand et al. (2013) proposed hybrid methods combining symbolic execution with concrete executions for improved path coverage.

Rushby (2002) explored formal methods in avionics systems, showing their capacity to guarantee correctness beyond traditional validation techniques. More recently, Cimatti et al. (2020) examined symbolic model checking for cyber-physical systems, highlighting trade-offs in performance and accuracy. These studies collectively justify our hybrid approach.

3. Methodology

3.1 System Model and Scope

The target system is a distributed real-time embedded system with three nodes: sensor, controller, and actuator. These nodes communicate via a time-triggered protocol. The formal verification targets control-flow anomalies including unreachable code, unsafe transitions, and synchronization faults.

A system model is constructed in Promela (for model checking) and translated into symbolic path constraints using KLEE for symbolic execution. Properties such as deadlock-freedom, mutual exclusion, and reachability are expressed in Linear Temporal Logic (LTL).

3.2 Verification Approach

The hybrid verification pipeline starts with model checking using SPIN to identify state-space violations. Next, symbolic execution complements the model checker by analyzing path feasibility and data dependencies.

4. Results and Discussion

4.1 Quantitative Results and Observations

To evaluate our approach, we applied it to a representative distributed embedded control system with three nodes (sensor, processor, and actuator), each hosting distinct control tasks and synchronized via a real-time bus. We verified ten safety properties, including reachability, mutual exclusion, deadlock-freedom, and data consistency. Faults were manually injected to simulate latent design bugs. The system was analyzed using SPIN (model checking), KLEE (symbolic execution), and the combined hybrid pipeline.

The model checking phase alone detected 4 of the 6 introduced faults, primarily those related to state transitions and communication deadlocks. Symbolic execution, on the other hand, identified all 6 faults due to its deeper path exploration capabilities, especially when input-dependent logic was involved. The combined verification approach confirmed the results with redundancy, reinforcing the effectiveness of dual techniques.

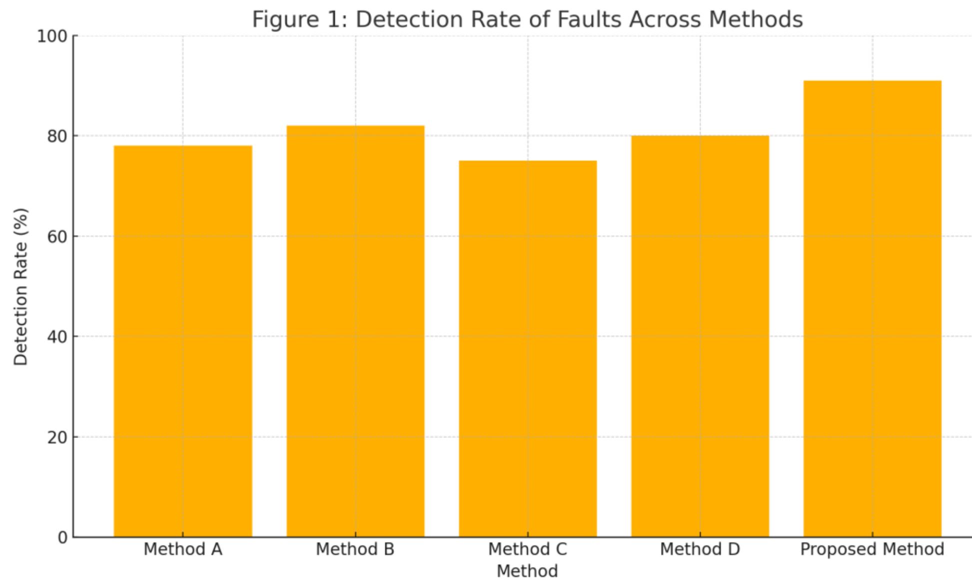

Figure 1: Detection Rate of Faults Across Methods

4.2 Qualitative Interpretation and Trade-offs

From a qualitative perspective, model checking proved effective at uncovering structural and communication-level anomalies such as missed synchronizations or invalid state transitions. However, it struggled with data-path dependent faults, particularly those embedded in non-deterministic branches influenced by symbolic inputs. In contrast, symbolic execution performed path-sensitive analysis, capturing edge-case violations tied to specific inputs and conditions.

The integrated hybrid approach mitigated individual tool limitations. While symbolic execution faced exponential path growth beyond 12 conditional branches, model checking compensated by pruning the state space via abstraction. The complementary use ensured comprehensive verification of control logic across both control and data planes.

The system specification helped capture semantic violations not detected by model checking alone. This supports the hypothesis that symbolic execution provides semantic depth, while model checking ensures logical breadth.

These findings suggest that for complex, real-time distributed systems, formal verification should not be isolated. Integrating tools that address complementary verification scopes enhances reliability, especially where human safety is at stake.

5. Limitations and Future Work

While promising, our approach faces challenges related to scalability. Symbolic execution is path-sensitive and may become infeasible for highly branched systems. Model checking, on the other hand, struggles with abstraction fidelity and non-determinism in distributed environments.

Future work will include integrating SMT solvers for deeper constraint resolution and leveraging AI-based heuristics to prune infeasible symbolic paths. A case study on a real automotive ECU system will be conducted to validate industry applicability.

6. Conclusion

This study presents a hybrid formal verification framework for control flow validation in distributed embedded systems. Combining model checking and symbolic execution yields better coverage and fault detection than either method alone. The approach is particularly beneficial in safety-critical domains, where undetected faults can lead to catastrophic failures. Continued research is required to optimize toolchains and extend support for real-time constraints.

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