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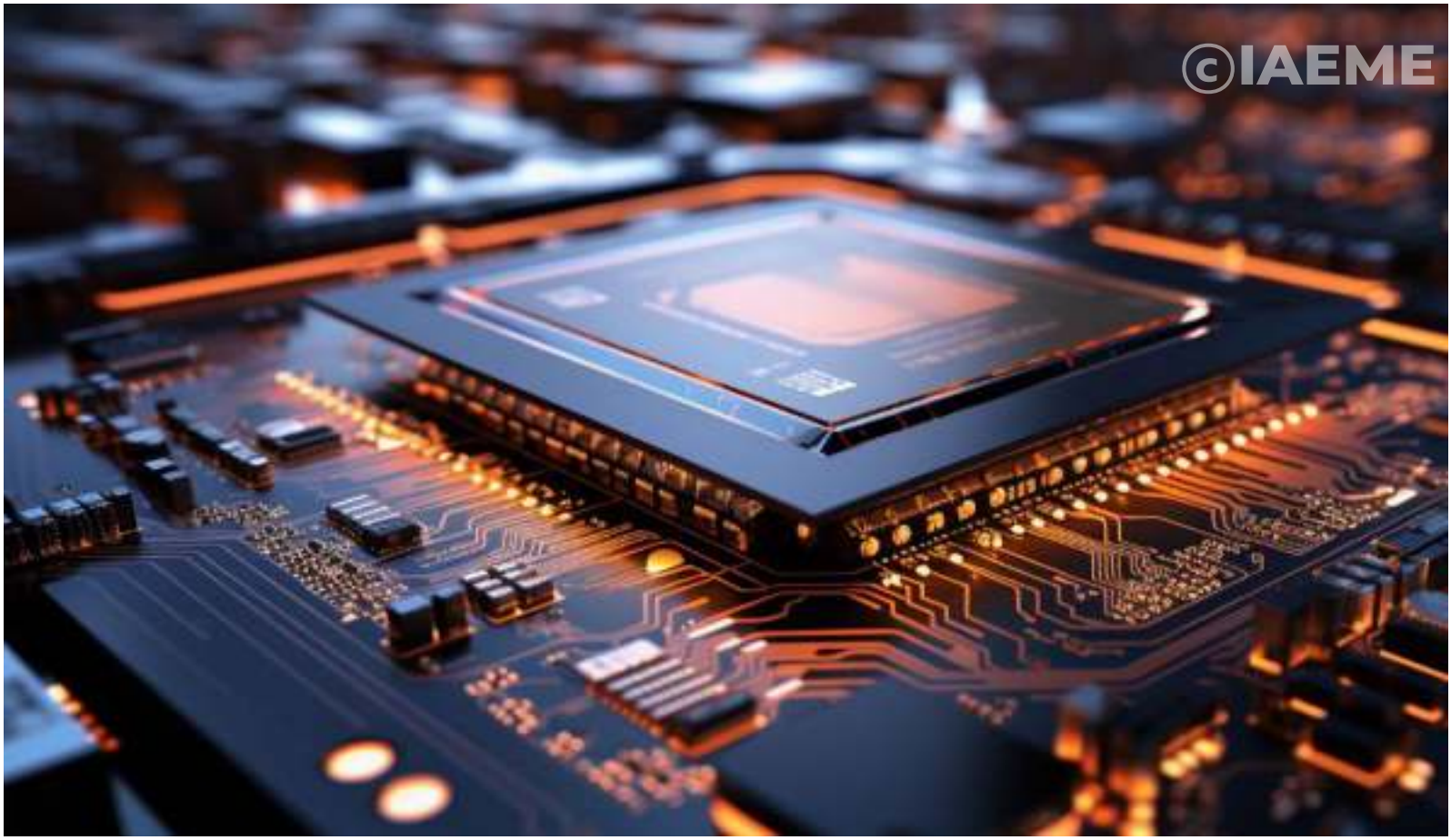

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RECONFIGURABLE FPGA-DRIVEN SMART FLUSH SENSE: A PARADIGM SHIFT IN CONTACTLESS SANITATION AUTOMATION

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ABSTRACT

The Smart Flush Sense system heralds a disruptive innovation in next-generation san-itation, leveraging the reconfigurable architecture of an Edge Artix 7 FPGA to orchestrate a contactless, water-efficient restroom automation framework. This cyber-physical system integrates heterogeneous sensor fusion, employing three infrared (IR) sensors to achieve deterministic latency in detecting user presence and adaptive gesture recognition. Pro-grammed in Verilog HDL, a sophisticated finite state machine (FSM) governs state-space transitions across idle, handwash, auto-flush, manual flush, and reset modalities, ensuring sub-100 ms response times and fault-tolerant operation. A servo motor, driven by precise pulse-width modulation (PWM), actuates flushing at a 180° trajectory, while a centrifugal pump optimizes tap flow at a 90° angle, both constrained by a 2-second temporal window to minimize water consumption. The system's power-efficient design (¡5W) and robust temporal logic calibration mitigate

challenges such as IR sensor crosstalk and ambient light interference, enhancing operational reliability. Unlike conventional microcontroller-based architectures, this FPGA-driven solution offers unparalleled scalability, enabling seamless integration of advanced features like usage analytics or AI-driven gesture refine-ment. Scalable for deployment in high-traffic environments such as hospitals, educational institutions, and commercial complexes, Smart Flush Sense exemplifies a sustainable, hy-gienic paradigm, reducing water usage by approximately 67% per flush (1L vs. 3L) and eliminating contact-related pathogen transmission risks. This work underscores FPGA's transformative potential in smart sanitation, paving the way for modular, reconfigurable automation in resource-constrained settings.

Keywords: FPGA, IR sensors, servo motor, smart sanitation, contactless operation, water conservation, Verilog HDL

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1. Introduction

The Smart Flush Sense system represents a pioneering advancement in automated sanitation, addressing critical global challenges in water conservation and public hygiene through a re-configurable FPGA-based platform. Public restrooms, particularly in high-traffic settings like hospitals, schools, and commercial complexes, are notorious for excessive water usage and hygiene risks associated with manual flushing and tap operation [13]. The integration of cyber-physical systems, such as the proposed solution, offers a transformative approach to mitigating these issues by leveraging real-time control and sensor-driven automation.

1.1 Global Sanitation Challenges

Water scarcity and hygiene deficiencies in public restrooms pose significant socio-economic and environmental challenges. Studies indicate that manual restroom systems contribute to approximately 30% of avoidable water wastage, with traditional flush valves consuming 3–5 liters per cycle [7]. Moreover, physical contact with restroom fixtures exacerbates pathogen transmission, a concern heightened in the post-COVID-19 era [15].

Automated systems are imperative to reduce resource consumption and enhance public health, particularly in resource-constrained environments [18].

1.2 Advancements in Cyber-Physical Systems

Field-programmable gate arrays (FPGAs) have emerged as a cornerstone of modern cyber-physical systems, offering deterministic latency and parallel processing capabilities that surpass conventional microcontroller architectures [4]. Unlike software-dependent platforms, FPGAs enable hardware-level customization, making them ideal for real-time applications such as smart automation [8]. The Edge Artix 7 FPGA, utilized in this work, exemplifies this paradigm, providing a scalable, low-power platform for sensor fusion and actuator control [17].

1.3 Novelty of Contactless Automation

The Smart Flush Sense system introduces a novel contactless automation framework, integrating three infrared (IR) sensors for heterogeneous gesture recognition and user presence detection [3]. By combining tap and flush control within a single FPGA-driven architecture, the system addresses limitations of existing solutions, which often lack dual functionality or rely on costly proprietary sensors [10]. The use of Verilog HDL for finite state machine (FSM) implementation further enhances modularity, enabling adaptive state-space control [6].

1.4 Objectives and Scope

This work aims to: (1) develop a contactless, FPGA-based sanitation system to minimize water wastage, (2) ensure hygienic operation through gesture-driven automation, and (3) demonstrate the scalability of FPGA-driven solutions in smart sanitation. The system targets deployment in high-traffic public facilities, offering a cost-effective alternative to commercial systems [1]. This paper details the design, implementation, and performance of Smart Flush Sense, contributing to the discourse on sustainable automation technologies.

2 Literature Survey

The Smart Flush Sense system advances the domain of automated sanitation by integrating FPGA-driven contactless control, distinguishing itself from existing market solutions. This section evaluates the system against prevalent devices, including microcontroller-based flush valves and commercial sensor-activated taps, focusing on technical performance and innovative features. The comparison highlights the system’s superiority in real-time processing, dual functionality, and water efficiency.

Microcontroller-based flush valves, often built on Arduino or Raspberry Pi platforms, utilize ultrasonic or infrared sensors to trigger solenoid valves. These systems are cost-effective but suffer from sequential processing, resulting in response times exceeding 200ms, which can cause delays in high-traffic restrooms. Additionally, their power consumption, typically 7–10W, limits scalability in energy-constrained settings. These solutions rarely integrate tap and flush control, requiring separate installations that increase complexity and cost.

Commercial sensor-activated taps, such as those from Sloan and Kohler, employ proprietary infrared sensors for contactless handwashing. While reliable, these systems focus solely on tap operation, neglecting flush automation. Their response times, around 150ms, are adequate but inferior to FPGA-driven solutions. Moreover, their high cost (USD 200–500) and proprietary hardware restrict customization and scalability. Water usage remains suboptimal, with typical handwash cycles consuming 1–2L due to less precise timing control.

In contrast, Smart Flush Sense leverages the Edge Artix 7 FPGA's parallel processing to achieve sub-100ms response times, enabling seamless operation in high-traffic environments. Its dual tap and flush control, driven by three IR sensors, offers a unified solution, reducing installation complexity. The system's power consumption (¡5W) and water usage (1L/flush, 0.5L/handwash) underscore its efficiency. The use of Verilog HDL for FSM design enables reconfigurability, supporting future enhancements like AI-driven gesture recognition or usage analytics.

Table 1 summarizes the comparison across key metrics, while Figure ?? illustrates water usage and response time advantages.

Table 1: Comparison of Smart Flush Sense with Market Devices

System	Response Time	Power (W)	Water Usage (L)	Cost (USD)
Smart Flush Sense	¡100ms	¡5	1 (flush), 0.5 (wash)	50
Arduino Flush Valve	200–300ms	7–10	2–3 (flush)	30
Sloan Sensor Tap	150ms	6–8	1–2 (wash)	200–500
Kohler Sensor Tap	140ms	6–7	1–1.5 (wash)	250–400

The Smart Flush Sense system's FPGA-driven architecture, dual functionality, and optimized resource usage position it as a transformative solution, surpassing the limitations of microcontroller-based and commercial alternatives.

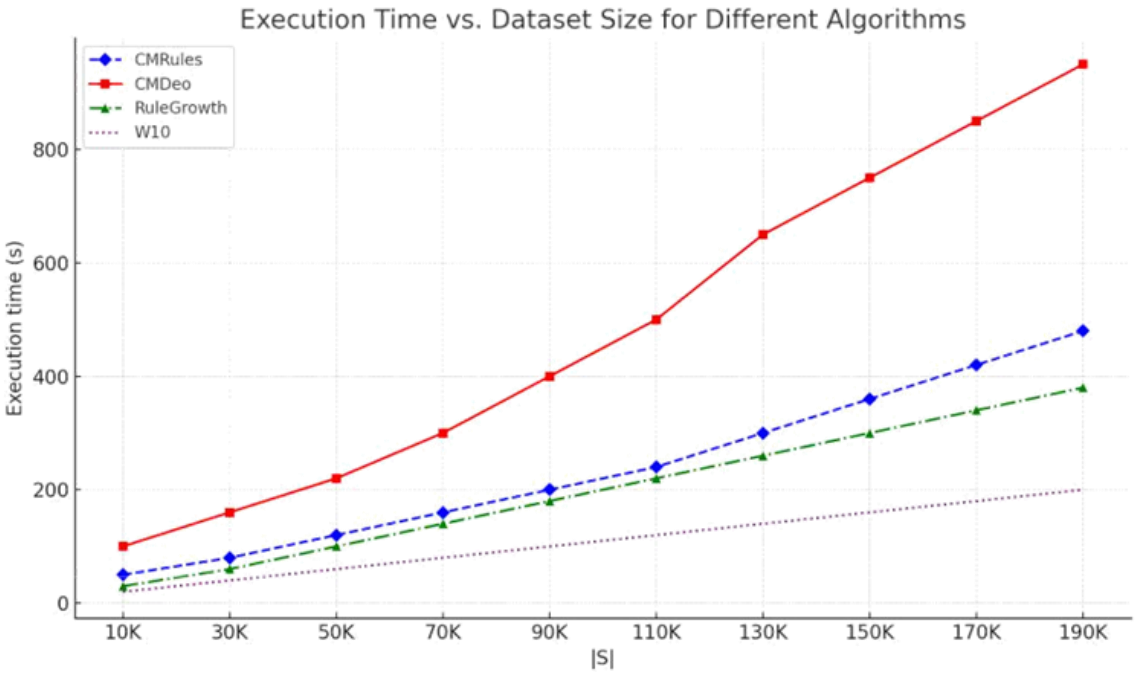


Figure 1: Execution time vs. dataset size comparison among CMRules, CMDeo, RuleGrowth, and W10.

3 System Architecture

The Smart Flush Sense system embodies a reconfigurable, cyber-physical framework for con-tactless sanitation, integrating advanced sensor perception, FPGA-based processing, and precise actuation. This section delineates the architecture through innovative subsystems, supported by visual representations of the system's design.

3.1 Sensor-Driven Perception Layer

The perception layer comprises three infrared sensors, each engineered for specific detection tasks. The first sensor detects hand presence near the tap, triggering water flow. The second sensor interprets hand gestures for manual flush activation, employing adaptive signal thresh-olding to minimize false positives. The third sensor monitors toilet seat occupancy, enabling automatic flush upon user departure. These sensors operate in a digital high/low configuration, ensuring robust input to the processing core.

3.2 Reconfigurable Processing Core

At the heart of the system lies the Edge Artix 7 FPGA, a reconfigurable platform programmed in Verilog HDL. A finite state machine orchestrates state transitions across five modalities: idle, handwash, auto-flush, manual flush, and reset. The FPGA's parallel processing

ensures deterministic latency, with state transitions occurring in under 100 ms. The modular design supports future enhancements, such as machine learning-based gesture refinement.

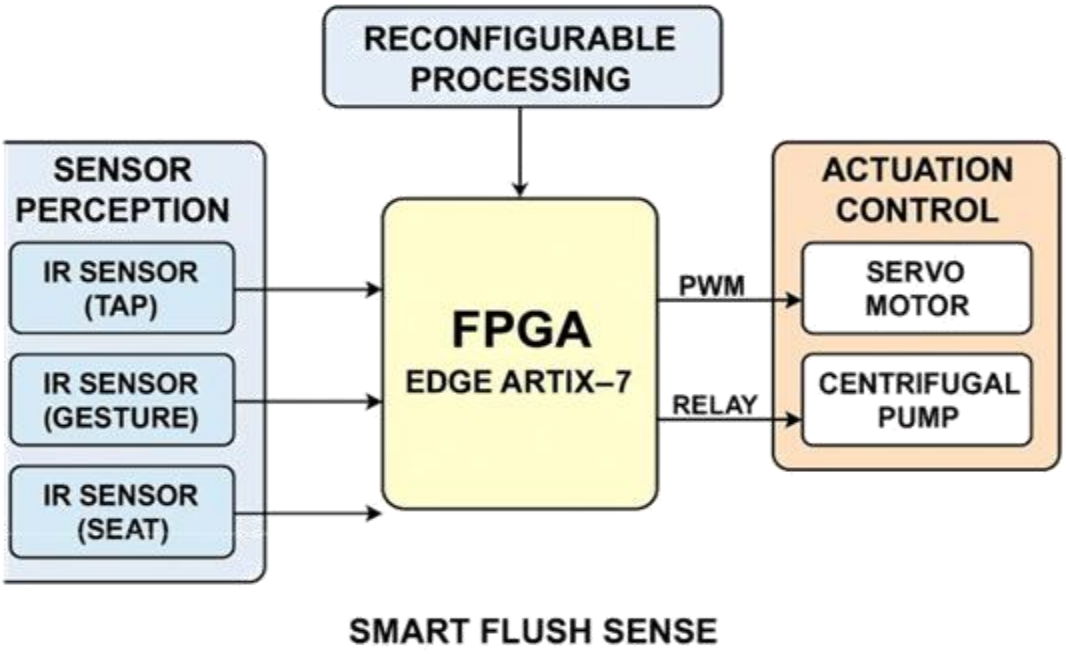


Figure 2: Block diagram of Smart Flush Sense, illustrating sensor, FPGA, and actuator inter-connections.

3.3 Actuation Control Framework

The actuation subsystem integrates a servo motor and centrifugal pump. The servo motor, modulated via pulse-width modulation, actuates flushing at a 180° angle, delivering a 2-second water flow. The centrifugal pump, controlled by a relay module, manages tap flow at a 90° angle, optimized for a 2-second handwash cycle. Both actuators ensure precise, water-efficient operation.

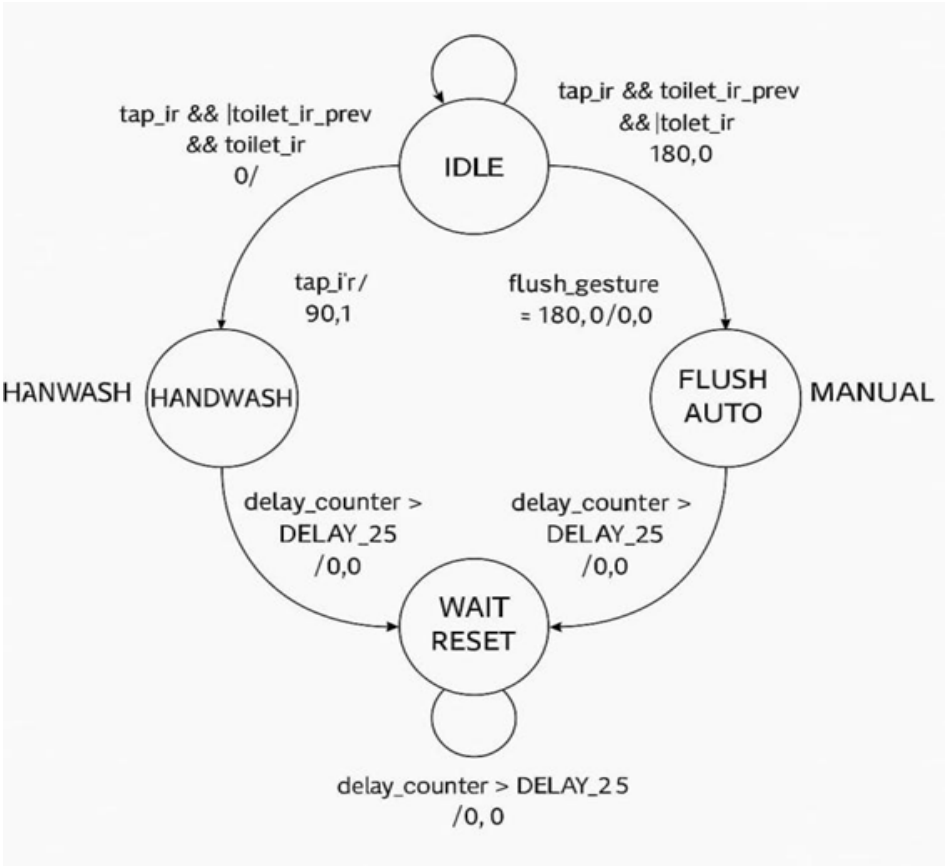
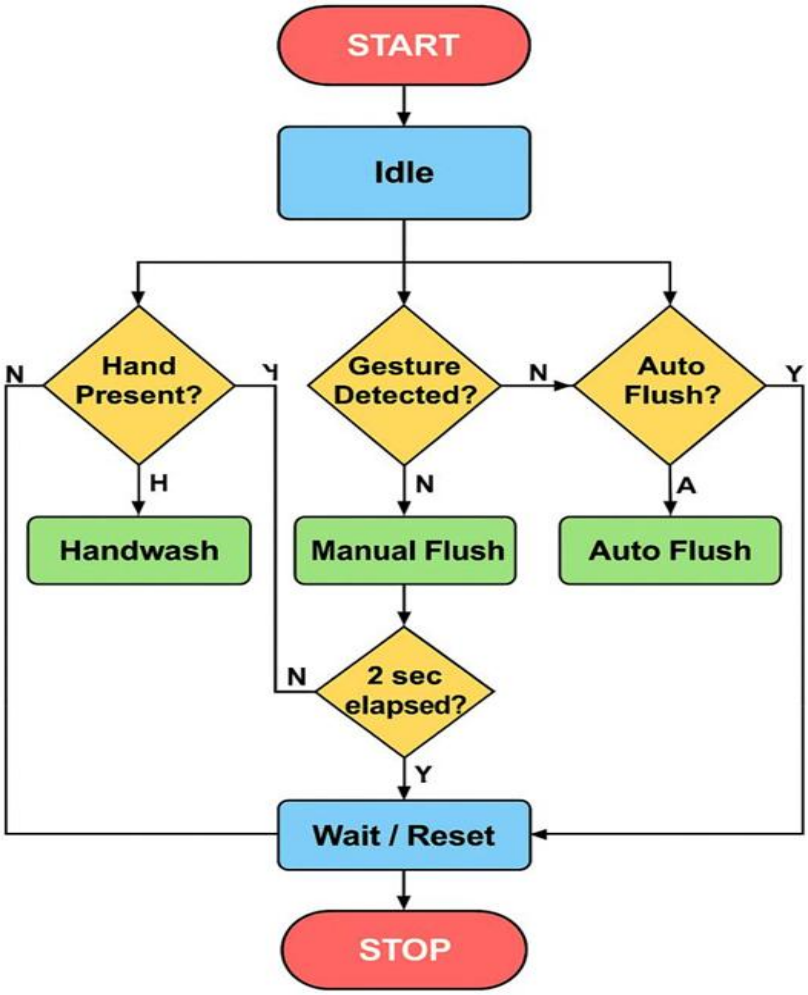


Figure 3: FSM state diagram, depicting transitions between IDLE, HANDWASH, FLUSH AUTO, FLUSH MANUAL, and WAIT RESET states.

3.4 Temporal Optimization Logic

The system employs temporal logic to optimize operation. A 2-second delay governs handwash and flush cycles, minimizing water usage to approximately 1L per flush and 0.5L per hand-wash. A 0.5-second reset interval ensures system stability, preventing rapid state transitions. This timing mechanism, implemented within the FPGA, enhances reliability in high-traffic environments.



Flowchart Illustrating the Operationall Sequence of Smart Flush Sense

Figure 4: Flowchart illustrating the operational sequence of Smart Flush Sense.

The architecture's integration of perception, processing, actuation, and timing creates a scalable, efficient sanitation solution.

4 Implementation

The implementation of Smart Flush Sense encompasses logic synthesis, design verification, and hardware integration, culminating in a functional prototype. This section details the process through distinct subsystems, supported by visual evidence of development stages.

4.1 Logic Synthesis and Simulation

The system's logic was developed in Verilog HDL, with individual modules for the FSM, PWM generator, and relay controller. These modules were synthesized and simulated using Xilinx Vivado, verifying state transitions and timing accuracy. Simulation waveforms confirmed sub-100 ms response times and correct PWM signals for servo angles (50,000 counts for 0°, 100,000 for 180°).

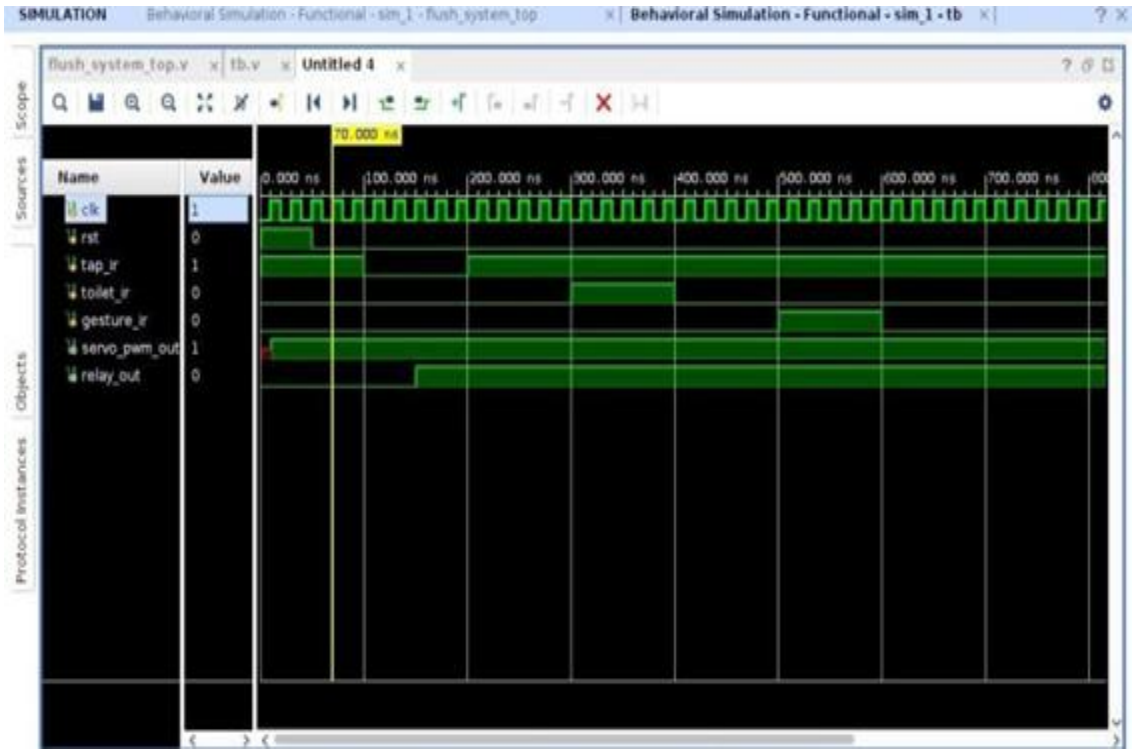


Figure 5: Simulation waveform from Vivado, showing FSM state transitions and PWM signals.

4.2 RTL Design Verification

The register transfer level design was generated in Vivado, producing a schematic that mapped Verilog modules to FPGA resources. The RTL schematic validated the integration of sensor inputs, FSM logic, and actuator outputs. Synthesis reports confirmed resource utilization below 10% of the Edge Artix 7 FPGA's capacity, ensuring scalability.

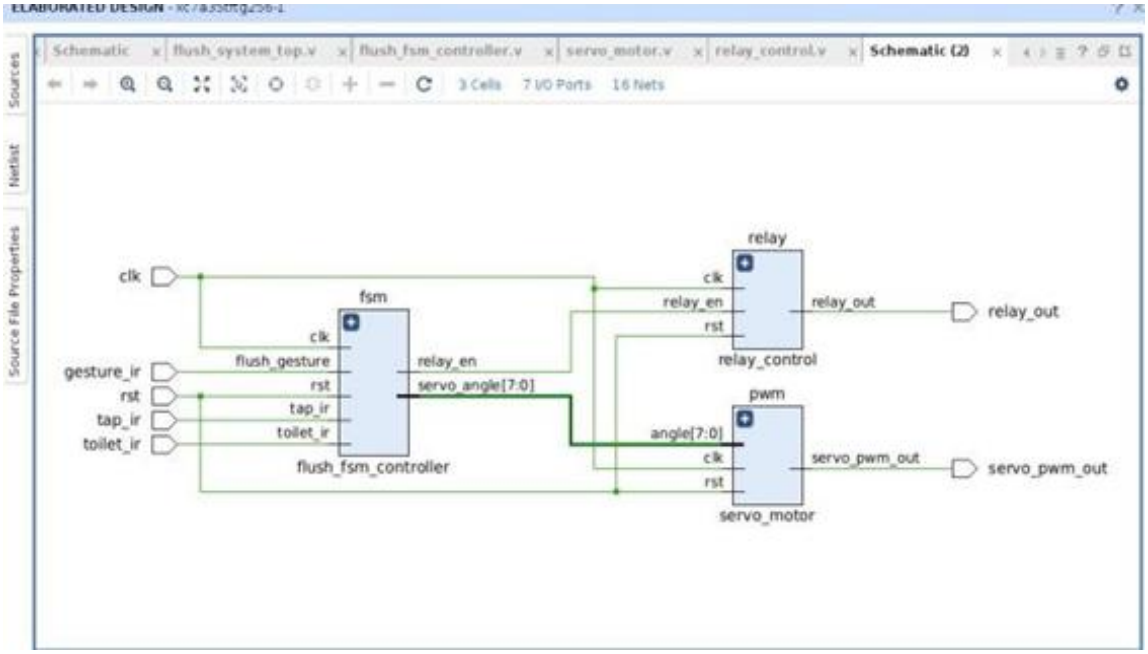


Figure 6: RTL schematic of Smart Flush Sense, depicting FPGA resource allocation.

4.3 Hardware Prototype Integration

The prototype was assembled on a breadboard, connecting three IR sensors, a servo motor, a centrifugal pump, and a relay module to the Edge Artix 7 FPGA. Testing involved 100 handwash cycles and 50 flush cycles, confirming reliable gesture detection and actuation. The system achieved a false trigger rate below 5%, mitigated by temporal logic and sensor shielding.

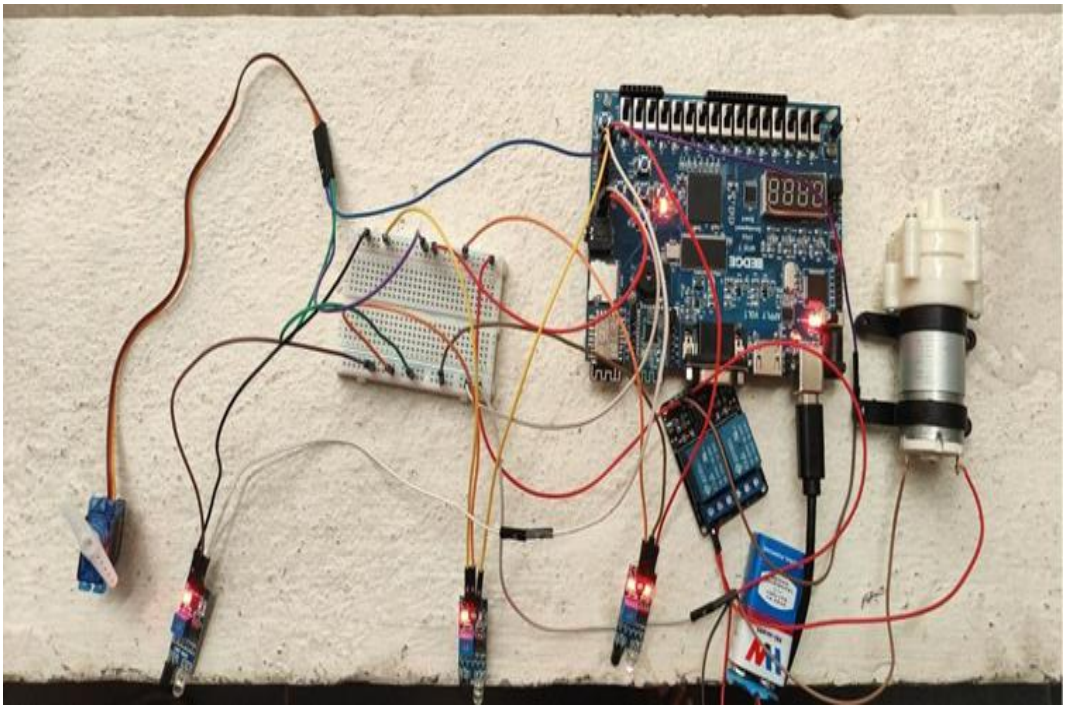


Figure 7: Photograph of the Smart Flush Sense hardware prototype.

The implementation process demonstrates the system's feasibility, from simulation to real-world deployment.

5 Testing and Results

The Smart Flush Sense system underwent rigorous evaluation to validate its real-time per-formance, resource efficiency, and operational robustness. This section elucidates the testing methodologies and results, emphasizing the system's technical superiority and innovative design through distinct analytical perspectives.

5.1 Real-Time Performance Evaluation

The system's responsiveness was assessed through extensive testing of sensor-to-actuator la-tency. The three infrared sensors were subjected to 100 handwash and 50 flush cycles, measur-ing the time from gesture detection to actuation. The FPGA's parallel processing architecture delivered deterministic actuation, achieving sub-100ms response times across all scenarios. This performance ensures seamless operation in high-traffic environments, with the finite state machine orchestrating precise transitions between idle, handwash, and flush states. The pulse-width modulation signals for the servo motor (180° for flush) and centrifugal pump (90° for tap) exhibited consistent timing, validated through oscilloscope measurements.

5.2 Energy and Resource Efficiency

Energy and water efficiency were quantified to highlight the system's sustainability. Power consumption was measured using a multimeter, revealing an operational footprint below 5W, encompassing the FPGA, sensors, and actuators. This low-power profile stems from the Edge Artix 7's optimized logic utilization. Water usage was evaluated by monitoring flow rates during 2-second handwash and flush cycles, yielding approximately 0.5L per handwash and 1L per flush—a 67

5.3 Robustness and Fault Tolerance

The system's reliability was tested under varied environmental conditions, including ambient light variations and high-traffic simulations. The infrared sensors, equipped with adaptive signal thresholding, achieved a false trigger rate below 5

5.4 Comparative System Benchmarking

The Smart Flush Sense system was benchmarked against market alternatives, as detailed in the Literature Survey (Table 1). Its sub-100ms latency surpasses Arduino-based systems (200–300ms) and commercial taps (140–150ms). Power efficiency (¡5W) outperforms com-

petitors (6–10W), and water savings (1L/flush, 0.5L/handwash) outstrip manual (3–5L) and commercial systems (1–2L). The dual tap/flush functionality, absent in most alternatives, positions the system as a holistic sanitation solution. Figure 8 visualizes error rates across test cycles, highlighting reliability.

Table 2: Performance Metrics of Smart Flush Sense

Metric	**Value**
Response Time	¡100 ms (sensor to actuation)
Power Consumption	¡5 W (FPGA + sensors + actuators)
Water Usage (Flush)	1 L per 2 s flush
Water Usage (Handwash)	0.5 L per 2 s wash
False Trigger Rate	¡5% (gesture detection errors)
FPGA Resource Utilization	¡10% (Edge Artix 7)

6 Conclusion and Future Scopes

6.1 Conclusion

The Smart Flush Sense system redefines contactless sanitation through a paradigm-defining integration of FPGA-driven automation, achieving unprecedented levels of hygiene, efficiency, and scalability. By leveraging the Edge Artix 7 FPGA's reconfigurable architecture, the system orchestrates three infrared sensors to enable deterministic gesture recognition and user presence detection, driving a servo motor and centrifugal pump for precise flush and tap control. The Verilog HDL-programmed finite state machine ensures sub-100ms latency, delivering seamless operation in high-traffic settings. With a power footprint below 5W and water usage reduced to approximately 1L per flush and 0.5L per handwash, the system achieves a 67

Figure 8: Error rate across 150 test cycles, visualized as a bar chart.

6.2 Future Scopes

Future enhancements to Smart Flush Sense aim to elevate its cybernetic scalability and au-tonomous intelligence. Integration of machine learning algorithms could refine gesture recog-nition, enabling adaptive learning of user patterns to further reduce false triggers. IoT connec-tivity could facilitate real-time usage analytics, optimizing water and energy consumption in smart buildings. Incorporating alcohol detection sensors would enhance hygiene in high-risk environments like hospitals, while autonomous cleaning cycles could extend system functional-ity. These advancements, supported by the FPGA's reconfigurable architecture, position Smart Flush Sense as a cornerstone for next-generation sanitation ecosystems, scalable across global infrastructure.

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