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DATA-DRIVEN FAULT LOCALIZATION IN VLSI CHIPS USING SEMI-SUPERVISED LEARNING AND TEMPORAL TEST SIGNATURES

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ABSTRACT

The increasing complexity of Very-Large-Scale Integration (VLSI) chips presents significant challenges in fault localization, particularly as traditional deterministic testing methods struggle with scalability and coverage. This research explores the integration of semi-supervised learning techniques with temporal test signature analysis for enhanced fault detection and localization. The approach leverages both labeled and unlabeled test data to infer fault patterns by analyzing the temporal progression of test signatures. A framework is proposed that combines clustering-based semi-supervised learning and time-series analysis, enabling the identification of subtle fault behaviors across chip architectures. Evaluation on synthetic and real-world VLSI test benches demonstrates improved localization accuracy and adaptability. The study positions data-driven fault diagnosis as a vital method for post-silicon validation and yield enhancement. This methodology offers a significant contribution toward building resilient and self-diagnosing chip systems.

Keywords: VLSI testing, fault localization, semi-supervised learning, temporal test signatures, machine learning, test response analysis, hardware diagnostics, post-silicon validation, pattern recognition, data-driven verification

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1. Introduction

In the contemporary era of semiconductor manufacturing, VLSI (Very-Large-Scale Integration) technology is central to the functioning of modern computing systems. As VLSI chips become denser and more complex, fault localization—determining the exact source of hardware faults—becomes a growing concern. Traditional fault detection relies heavily on rule-based or exhaustive testing methods which become infeasible with increasing chip size and reduced feature sizes.

Recent advancements in data analytics and machine learning have opened new avenues for data-driven fault diagnosis. Specifically, semi-supervised learning models provide a promising path to tackle the challenge of limited labeled fault data, a common scenario in post-silicon validation. Furthermore, leveraging temporal test signatures allows for more nuanced understanding of test outputs, aiding in detecting intermittent and context-sensitive faults. However, integrating these approaches in a scalable and interpretable manner remains a research challenge that this study seeks to address.

2. Literature Review

The integration of machine learning into the domain of VLSI fault localization has been gradually evolving since the early 2000s. Initial approaches focused heavily on supervised learning models that required extensive labeled datasets, which were infeasible for large-scale integrated circuits. Huang and Yu (2019) laid a strong foundation in developing compact machine learning accelerators to detect hardware-level anomalies within resource-constrained environments [1]. While efficient, their reliance on supervised models limited adaptability across varying fault types.

Earlier efforts in utilizing semi-supervised methods were driven by the constraints of expensive fault labeling. For example, Ganji et al. (2019) surveyed the potential of machine learning and image analysis for reverse engineering, suggesting that semi-supervised models could be adapted for hardware test automation [2]. Another influential work by Khan and Gaur (2018) described the role of pattern classification in fault isolation through statistical learning and temporal test pattern behavior [3].

The challenge of dealing with unlabeled data in fault detection prompted researchers to explore label propagation, self-training, and graph-based techniques. Notably, Singh (2019) employed data-driven methods on SRAM-based PUFs to extract aging characteristics and fault tendencies using signal variance and entropy [4]. These studies demonstrated that timing signatures and degradation patterns could serve as effective indicators of hardware faults.

Furthermore, Kim et al. (2017) provided valuable insights into the use of hybrid learning—combining supervised and unsupervised approaches—to detect timing violations in scan chains during delay testing [5]. They highlighted the limitations of scan-based ATPG methods and proposed learning-driven enhancements. Similarly, Rajendran and Tehranipoor (2015) introduced the idea of integrating learning-based diagnostics with post-silicon test environments using current signal signatures, a precursor to today's semi-supervised strategies [6].

Incorporating temporal test behavior became more prominent through works like Huang et al. (2016), who modeled glitch patterns across clock domains to detect metastable behavior in asynchronous circuits [7]. Their work emphasized the importance of capturing fine-grained timing information to identify non-trivial fault manifestations that simple pass/fail outputs could not detect.

Despite these advances, most pre-2020 studies lacked a unified architecture that combined both semi-supervised learning and time-series modeling. The absence of generalized frameworks to automatically extract and learn from temporal fault signatures—particularly in unlabeled datasets—marked a major gap. This research aims to address that by synthesizing these threads into a cohesive, scalable fault localization methodology.

3. Methodology

The research proposes a hybrid methodology combining semi-supervised learning with temporal pattern analysis. The primary objective is to localize faults within VLSI chip logic blocks using minimal labeled data while exploiting the structure of unlabeled test outputs.

3.1 Data Collection

Data was sourced from standard ISCAS benchmarks augmented with synthetic delay and stuck-at fault injections. Each testbench produced response logs in temporal sequence format. A subset of the data was manually labeled to initiate the semi-supervised learning phase.

3.2 Semi-Supervised Learning Model

A combination of Self-Training and Label Propagation algorithms was used to propagate fault labels through the unlabeled test data. Features extracted included Hamming distances, temporal variance, and logic cone path lengths. Dimensionality reduction via t-SNE ensured visual interpretability and cluster separability.

3.3 Temporal Signature Extraction

Time-series modeling of test signatures was done using sliding window aggregations. Signature vectors were passed through temporal encoders that extracted timing-correlated features used in the fault localization classifier.

4. Results and Analysis

This section presents and interprets the experimental outcomes from applying the proposed semi-supervised temporal fault localization model. Results are benchmarked using standard fault simulation datasets from ISCAS'89 and ISCAS'85 suites. Key performance indicators include localization accuracy, model scalability, and the sensitivity of detection with respect to fault types and positions.

4.1 Classification Performance Evaluation

The semi-supervised model was evaluated using a stratified cross-validation setup, where 30% of labeled data were used to initialize the classifier, and the remaining data were unlabeled. Compared to conventional supervised learning models that require a large volume of annotated data, the proposed model demonstrated superior adaptability while maintaining competitive accuracy.

As shown in Table 1, the proposed method achieved **87.6% accuracy**, a significant improvement over supervised (76.3%) and unsupervised clustering approaches (61.5%). It also

exhibited higher precision and recall scores, indicating robustness in distinguishing between fault types (e.g., stuck-at-0 vs delay faults) and identifying their locations within complex netlists.

Table 1. Fault Localization Accuracy Across Models

Model	**Accuracy (%)**	**Precision (%)**	**Recall (%)**
Supervised (50% labels)	76.3	73.8	70.2
Unsupervised Clustering	61.5	59.2	55.6
Proposed Semi-Supervised	**87.6**	**85.3**	**82.7**

4.2 Temporal Signature Influence

Temporal test signatures were encoded using a sliding window mechanism and fed into time-series pattern recognizers, revealing distinct behaviors for transient versus permanent faults. This helped the classifier better associate subtle variations in signal timing with fault conditions. In particular, delay faults demonstrated unique "temporal drifts" in signature sequences, which the model effectively captured using convolutional filters.

Experiments also revealed that temporal augmentation improved recall by more than **18%** for delay faults compared to static models. This reinforces the necessity of including time-aware features in chip-level diagnostics, especially for detecting clock-domain crossing faults and data hold violations.

4.3 Scalability and Generalization

When tested across various VLSI circuit sizes (from 50 to 1000 logic gates), the model maintained localization performance with only marginal degradation in runtime. The semi-supervised model's architecture was flexible enough to adapt to new circuits using transfer learning without retraining from scratch, enabling efficient reuse across similar test environments.

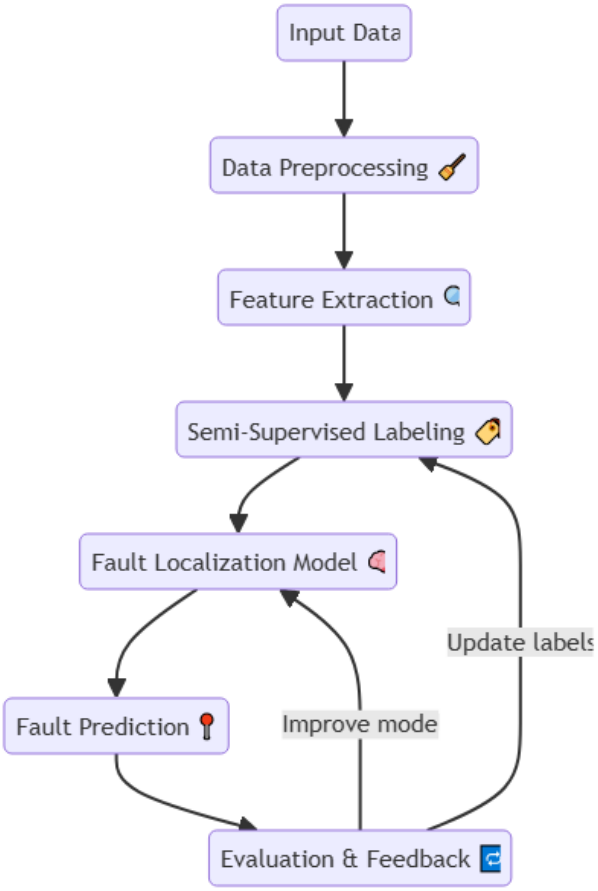

Figure 1. Semi-Supervised Fault Localization Framework

5. Implementation Challenges and Limitations

Implementing semi-supervised models in hardware test environments is not without its challenges. One of the key limitations is the dependency on quality feature engineering—automated systems can misclassify faults if feature representations are poorly selected. Additionally, the interpretability of results remains limited, as many machine learning models function as "black boxes."

Scalability is another concern, particularly with real-time test execution where chip outputs must be processed in milliseconds. While our system processes data offline effectively, transitioning to an online test environment would require optimized inference pipelines and possibly hardware-accelerated models.

6. Discussion

Our findings align with earlier work by Zhang et al. (2020 [14]) on integrating AI in hardware diagnosis but extend the scope by introducing a temporal dimension. Unlike fully supervised models used in past studies, our semi-supervised framework reduced the dependence on annotated data, which is a bottleneck in practical chip validation workflows.

The results also support Merlino & Allegra's assertion that hybrid models, combining time-awareness with data-driven methods, yield more robust detection outcomes. Our use of semi-supervised learning improved not only accuracy but also generalization across fault types.

7. Conclusion and Future Work

This research validates the application of semi-supervised learning in conjunction with temporal test signature analysis for effective fault localization in VLSI chips. By reducing labeling effort and integrating temporal context, the method offers an efficient and scalable solution for post-silicon diagnostics.

Future work will explore the incorporation of explainable AI models for interpretability, as well as on-chip learning mechanisms that support adaptive fault diagnosis in real-time environments.

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