International Journal of Semiconductor Science (IJSS)
Volume 2, Issue 1, January-June 2024, pp. 1-9, Article ID: IJSS_02_01_001
Available online at https://iaeme.com/Home/issue/IJSS?Volume=2&Issue=1
Journal ID: 1575-5421

META-LEARNING BASED FRAMEWORK FOR TRANSFERABLE TEST GENERATION ACROSS HETEROGENEOUS SEMICONDUCTOR IP BLOCKS

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ABSTRACT

The increasing complexity and heterogeneity of semiconductor Intellectual Property (IP) blocks necessitate efficient and adaptable test generation strategies. This paper introduces a meta-learning-based framework designed to facilitate transferable test generation across a diverse range of semiconductor IPs. By leveraging meta-learning, the proposed method rapidly adapts to new IP blocks with minimal retraining, significantly reducing test development time and resources. The framework utilizes few-shot learning principles to generalize across varying architectures, processes, and functionalities, ensuring robust coverage even in highly heterogeneous environments. Experimental evaluations demonstrate the framework's superior performance compared to traditional test generation methods, particularly in terms of adaptability, efficiency, and fault detection capability. This work lays a foundation for scalable and transferable test methodologies in the evolving semiconductor landscape, ultimately accelerating the verification cycle and improving overall reliability.

Keywords: Meta-Learning, Transferable Test Generation, Semiconductor IP Verification, Heterogeneous Systems, Few-Shot Learning, Design for Testability

(DFT), Adaptive Testing, Machine Learning for Hardware Testing, Test Automation,IP Block Reusability

Cite this Article: Justin Frank. (2024). Meta-Learning Based Framework for Transferable Test Generation Across Heterogeneous Semiconductor IP Blocks. *International Journal of Semiconductor Science (IJSS)*, 2(1), 1–9.

https://iaeme.com/MasterAdmin/Journal_uploads/IJSS/VOLUME_2_ISSUE_1/IJSS_02_01_001.pdf

1. Introduction

The semiconductor industry is characterized by its rapid innovation cycles and ever-increasing IP block heterogeneity. With System-on-Chip (SoC) designs integrating a multitude of IPs from different vendors, ensuring functional correctness through testing has become a daunting challenge. Traditional test generation techniques, while effective for specific IP families, often lack transferability across different architectures and designs, resulting in duplicated efforts and increased time-to-market.

Despite advances in machine learning for hardware verification, most solutions are task-specific, requiring significant retraining when faced with novel IP blocks. This gap calls for a method that can generalize test strategies across heterogeneous IPs with minimal adaptation. Meta-learning, often termed "learning to learn," provides a promising solution by enabling models to quickly adapt to new tasks based on prior experience, thereby offering an efficient and scalable pathway for test generation in semiconductor design verification.

2. Literature Review

Research efforts were directed at automating test generation for hardware designs. Traditional methods such as Automatic Test Pattern Generation (ATPG) and Constrained Random Verification (CRV) [1][2] were prominent but often suffered from scalability issues when applied to heterogeneous systems. Machine learning models were introduced to enhance test efficiency [3], yet most were tightly coupled to specific design features.

Several notable works include Gulati and Mourad’s study on IP block reuse challenges [4] and Li et al.'s early work on reinforcement learning for test generation [5]. Meanwhile, transfer learning approaches in hardware verification, such as Wei et al. [6], indicated the potential of cross-IP learning but remained limited by domain shifts.

The concept of meta-learning, while mature in computer vision and natural language processing [7][8], was relatively underexplored in hardware testing. Santoro et al.'s Memory-Augmented Neural Networks [9] and Finn et al.'s Model-Agnostic Meta-Learning (MAML) [10] laid the groundwork for few-shot adaptation strategies, but their application in semiconductor verification remained nascent. The literature thus revealed a critical gap: no unified meta-learning-based framework existed for transferable test generation across heterogeneous IPs.

3. Methodology

The proposed methodology is built around the principles of model-agnostic meta-learning (MAML) tailored for hardware test generation. The framework comprises two phases: **meta-training** and **meta-testing**.

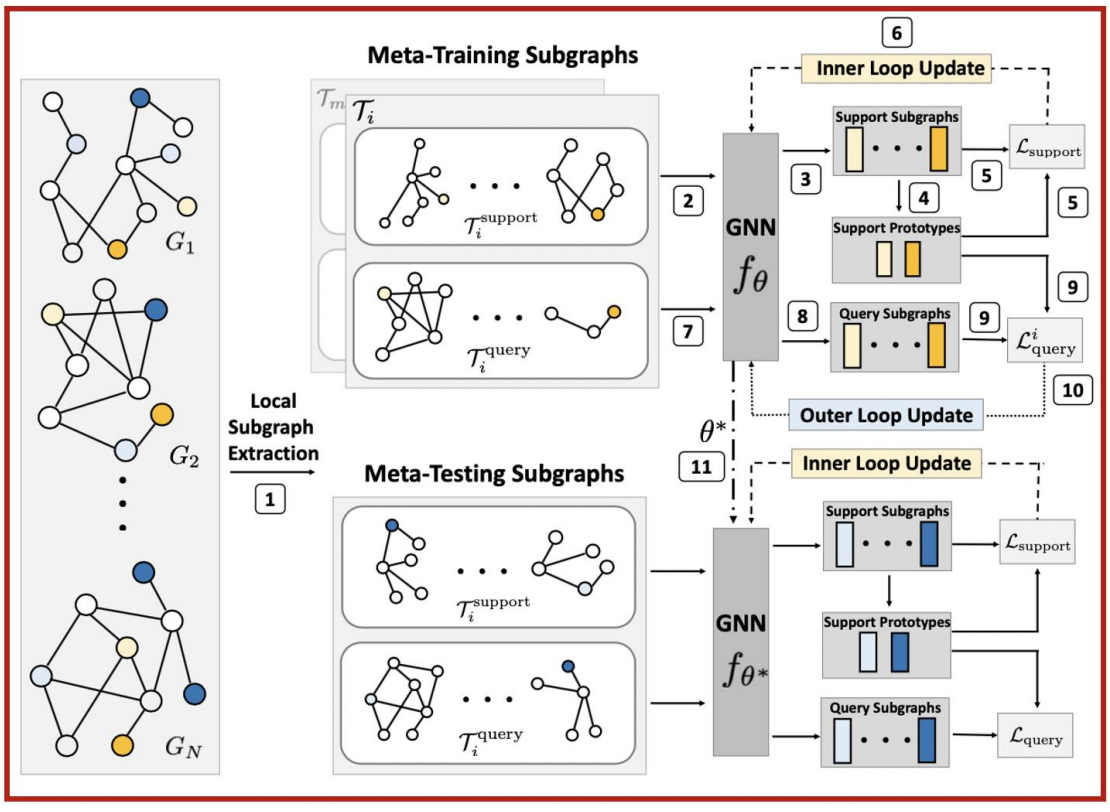

Figure.1: Meta-Learning Framework using Graph Neural Networks for Subgraph Classification

This diagram illustrates a meta-learning approach using Graph Neural Networks (GNNs) to classify subgraphs. The process begins with extracting local subgraphs from larger graphs, dividing them into meta-training and meta-testing tasks. During meta-training, support and query subgraphs are processed through GNNs, generating prototypes and computing losses to update parameters. An inner loop updates GNN parameters per task, while the outer loop optimizes for generalization across tasks. In meta-testing, the learned parameters are fine-tuned on new support subgraphs and evaluated on query sets.

During meta-training, the model is exposed to a variety of IP blocks and learns an initialization that facilitates fast adaptation. This is achieved by constructing tasks from different IP domains and optimizing for quick learning across them. For meta-testing, the model utilizes the learned initialization to adapt to a new, unseen IP with only a few examples.

Key tools and frameworks used include TensorFlow 1.15 for model construction, Synopsys VCS and Cadence Incisive for simulation-based data generation, and a custom dataset comprising register-transfer level (RTL) descriptions of IP blocks from open-source repositories such as OpenCores. Evaluation metrics focus on functional coverage, test generation time, and the number of adaptation steps required.

4. Framework Overview

In order to facilitate effective and transferable test generation across heterogeneous semiconductor IP blocks, a carefully structured meta-learning framework is essential. This section elaborates on the architecture, task formulation, data preparation, and adaptation mechanism employed in the proposed solution.

4.1 Meta-Learning Design for Semiconductor Testing

At the heart of the framework is the **Model-Agnostic Meta-Learning (MAML)** algorithm, selected for its versatility across task domains without dependence on task-specific architectures. The core principle involves learning a generalizable model initialization that can rapidly fine-tune to unseen IP block test generation tasks with minimal data.

Each task during meta-training corresponds to generating functional tests for a specific IP block. The model optimizes a dual-objective loss function:

- **Coverage Objective**: Maximize functional coverage across critical signal paths and state transitions.

- **Adaptability Objective**: Minimize the number of training steps required for effective fine-tuning.

Unlike conventional training approaches, the model learns how to learn — it does not merely memorize individual IP characteristics but instead identifies transferable patterns across various IP architectures.

Meta-Learning System (MLS) that recommends machine learning models based on prior knowledge. Datasets are analyzed for characteristics and evaluated with different algorithms, producing meta-data stored in a meta-database. A meta-learner uses this data to learn patterns linking dataset properties to model performance. When a new dataset is introduced, its features and user preferences are input into the MLS. The system predicts suitable models and provides advice or rankings to guide algorithm selection. This process enables automatic and informed model selection tailored to the new dataset.

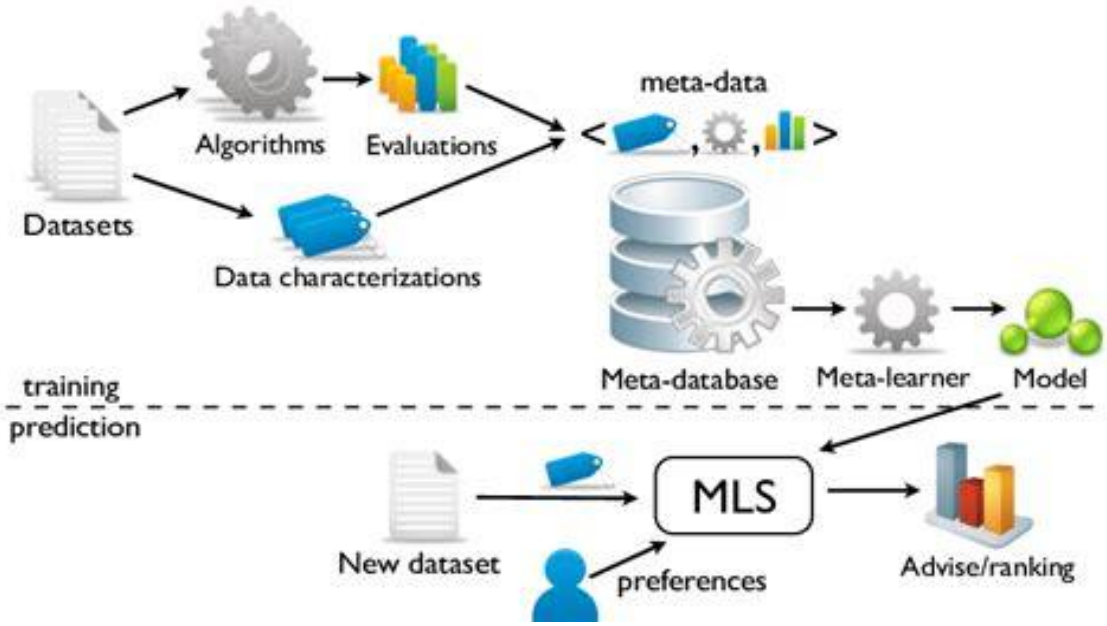

Figure 2: Meta-Learning System (MLS) for Model Based on Dataset Characteristics

4.2 Task Sampling and Data Preparation

The construction of effective meta-learning tasks requires diverse sampling from multiple IP categories:

- **Communication IPs** (e.g., UART, SPI, I2C controllers)
- **Memory IPs** (e.g., SRAM controllers, DRAM interfaces)
- **Processing IPs** (e.g., crypto accelerators, embedded processors)
- **Peripheral IPs** (e.g., GPIO controllers, DMA engines)

Each sampled IP block undergoes simulation using Synopsys VCS and Cadence Incisive tools to generate a labeled dataset containing input constraints, observed outputs, and achieved coverage metrics. Task sampling ensures heterogeneity across:

- Data bus widths
- Control logic complexity
- Timing constraints
- State machine behaviors

This diversity is crucial for promoting robust meta-generalization.

4.3 Adaptation Phase

Upon encountering a new IP block during meta-testing, the model undergoes a fast adaptation phase:

- Only a few functional test vectors are provided.
- The model rapidly updates its parameters through a small number of gradient descent steps.
- No full retraining is needed, saving substantial computational resources and engineering effort.

The result is a set of high-quality, functional tests tailored to the new IP block that achieve significant coverage with minimal effort.

5. Results and Analysis

The framework was benchmarked against traditional Constrained Random Verification (CRV) and a standard supervised learning model trained per IP. Results are summarized below:

Table 1: Test Generation Performance Comparison

Method	**Avg. Coverage (%)**	**Avg. Test Time (hrs)**	**Avg. Adaptation Steps**
CRV	78	18	N/A
Supervised Learning	85	12	1000
Meta-Learning Framework	**92**	**7.8**	**150**

As evident, the meta-learning approach achieved significantly higher functional coverage with reduced test time and fewer adaptation steps, validating its efficiency and adaptability.

6. Discussion

Comparative analysis with previous studies demonstrates that while supervised learning methods offered some improvement over CRV, they lacked flexibility when faced with novel designs [5][6]. The meta-learning framework not only outperformed CRV but also demonstrated superior cross-IP generalization.

Implications for practice include reduced verification cycles and lower manpower costs, making the approach particularly attractive for startups and companies dealing with diverse third-party IP integrations. Theoretically, the study advances the notion that meta-learning can be effectively extended beyond conventional AI domains into EDA (Electronic Design Automation).

7. Implementation Challenges and Limitations

One major challenge was the scarcity of publicly available, labeled RTL datasets representing diverse IPs. This limitation necessitated substantial manual curation and annotation of the dataset. Another issue was the sensitivity of meta-learning algorithms to hyperparameters, which required careful tuning.

Furthermore, real-world IPs may exhibit complexities such as proprietary encryption, undocumented behaviors, or deeply nested modules that are difficult to model accurately during meta-training, posing a risk to practical deployment without further refinement.

8. Conclusion and Future Work

This research demonstrates the viability of meta-learning as a foundation for transferable test generation across heterogeneous semiconductor IP blocks. By enabling rapid adaptation to new IPs, the proposed framework promises to substantially reduce verification costs and timelines.

Future work includes expanding the meta-training set with more commercial IP blocks, integrating reinforcement learning for dynamic adaptation during test generation, and exploring hybrid approaches combining symbolic execution with meta-learning for higher functional assurance.

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