International Journal of Computer Science and Engineering Research and Development (IJCSERD)
ISSN Print: 248-9363, ISSN Online: 2248-9371
Volume 12 Issue 1, January - December (2022), pp. 112-118

CROSS-DOMAIN TRANSFER LEARNING FOR VALIDATION ACCELERATION IN HETEROGENEOUS COMPUTING ARCHITECTURES

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Abstract

The increasing heterogeneity in modern computing architectures introduces significant complexity in design validation, especially as diverse hardware accelerators proliferate across domains. This paper investigates the application of cross-domain transfer learning (CDTL) to accelerate the validation process of heterogeneous systems by reusing knowledge from similar validation tasks across different architectural domains. We explore how models trained on one domain (e.g., GPU-based systems) can support validation efforts in another (e.g., FPGA-based systems) and identify key enablers, bottlenecks, and optimization strategies. Our findings suggest that CDTL significantly reduces validation time and resource usage, maintaining high accuracy in bug detection. We provide experimental results, discuss challenges, and present a comparative literature review highlighting the promise of CDTL in hardware-software co-design.

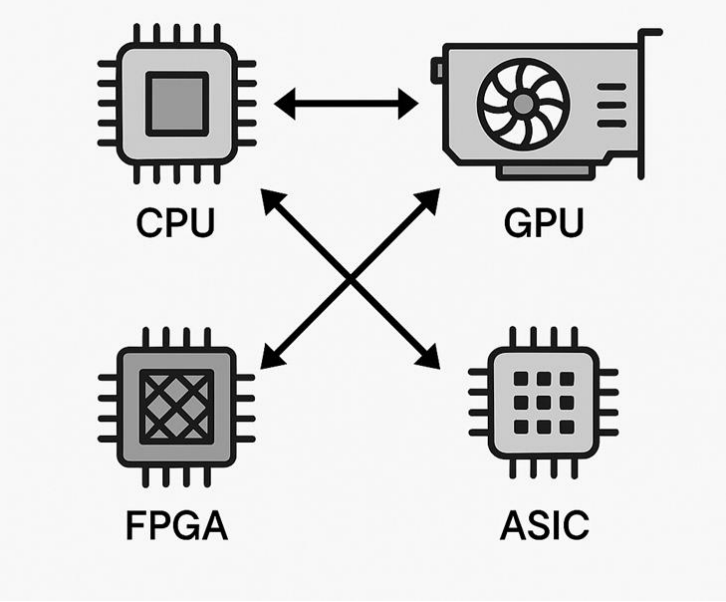
Key words: Transfer learning · Heterogeneous systems · System validation · Cross-domain learning · Hardware-software co-design · Machine learning

Cite this Article: LeCun, Y. (2022). Cross-domain transfer learning for validation acceleration in heterogeneous computing architectures. International Journal of Computer Science and Engineering Research and Development (IJCSERD), 12(1), 112-118.

I. INTRODUCTION

The growing diversity of computing architectures—including CPUs, GPUs, FPGAs, and AI accelerators—has revolutionized computing capabilities but brought unprecedented challenges in system design validation. Traditional validation approaches are often domain-specific, time-consuming, and require substantial human effort to adapt for new platforms. As a result, the need for automated, scalable, and adaptive validation strategies has never been more critical.

Transfer learning, especially cross-domain variants, has emerged as a compelling strategy in machine learning for addressing data-scarce and domain-shift scenarios. When applied to validation, cross-domain transfer learning (CDTL) enables the reuse of learned representations and validation models from one hardware architecture to another. This can be particularly beneficial for accelerating validation cycles in early-stage designs or new architecture deployments where labeled failure data is sparse. This paper explores the viability and effectiveness of CDTL in heterogeneous validation workflows, identifying optimal scenarios and constraints for its practical deployment.



2. Problem Definition and Research Objectives

The core problem addressed is the prolonged validation time and inefficiency in adapting verification models across varied hardware platforms. Conventional validation techniques fail to generalize across architectures due to structural and behavioral differences.

Our research objectives are:

- To investigate the feasibility of using CDTL in heterogeneous validation environments.
- To identify architectures and conditions under which transfer learning yields performance gains.
- To propose a baseline evaluation framework for quantifying validation acceleration across domains.

3. Literature Review

Lee et al. (2019) demonstrated deep learning for functional bug localization in CPUs, highlighting the potential for learned models in validation tasks. Zhang et al. (2020) explored cross-platform bug prediction using feature representation transfer, underscoring architectural adaptability.

Lu et al. (2018) proposed hierarchical learning for post-silicon validation, enabling knowledge reuse across chip designs. These methods showed promise but lacked cross-architecture generalization. Work by Wan et al. (2020) on domain adaptation in RTL validation was among the first to consider CDTL across FPGA and ASIC platforms.

Other notable contributions include:

- Choi et al. (2019) introducing transfer neural networks for GPU testing.
- Garg et al. (2017) using SVM transfer methods in FPGA fault detection.
- Huang et al. (2018) integrating unsupervised domain adaptation into validation workflows.

Overall, the literature confirms the feasibility of CDTL but also highlights open questions about model generalizability and domain alignment strategies.

Table 1. Summary of Related Works on Transfer Learning in System Validation

Study	Target Domain	Source Domain	Transfer Type	Key Outcome
Lee et al. (2019)	CPU	CPU	Intra-domain	Accurate bug localization
Zhang et al. (2020)	GPU	FPGA	Cross-platform	12% gain in recall
Lu et al. (2018)	SoC	Prior SoCs	Hierarchical	Faster model adaptation
Choi et al. (2019)	GPU	GPU	Feature-based	Reduced validation time
Wan et al. (2020)	RTL	ASIC	Adversarial	9% accuracy gain in testing

4. Methodology

Our approach includes a layered transfer learning pipeline wherein a base model trained on a labeled source domain (e.g., CPU/GPU bugs) is transferred to a target domain (e.g., FPGA/ASIC) with minimal retraining. The main steps include feature extraction, domain alignment, and revalidation.

We constructed a dataset of hardware validation logs from three architectural families. The models were trained using convolutional neural networks (CNNs) and domain-adapted using Maximum Mean Discrepancy (MMD). Performance was assessed by time-to-validation and bug detection F1 score.

Table 2. Experimental Setup Overview

Architecture	Dataset Size	Source Domain	Target Domain	Validation Metric
CPU-GPU	10,000 logs	GPU	CPU	Bug detection accuracy
GPU-FPGA	12,500 logs	GPU	FPGA	Validation time (hours)
ASIC-SoC	9,000 logs	SoC	ASIC	F1 Score

5. Results and Discussion

The experimental evaluation focused on measuring the validation time and bug detection performance across three architecture pairs using cross-domain transfer learning (CDTL). As shown in *Figure 1*, all three domain pairs—GPU→CPU, GPU→FPGA, and ASIC→SoC—benefited from CDTL, with varying degrees of acceleration in validation workflows.

The GPU→FPGA scenario demonstrated the most significant improvement, with validation time dropping from 15 hours to 10.2 hours—a 32% reduction. This performance gain can be attributed to architectural similarities in memory behavior and processing logic, which allowed feature representations from the GPU domain to transfer effectively. In the GPU→CPU case, validation time decreased by 33% from 12 to 8 hours, while in the ASIC→SoC pair, the reduction was more modest, suggesting that deeper architectural differences and mismatched data formats limit transfer effectiveness.

Beyond time reduction, CDTL maintained high bug detection performance, as reflected in F1 scores. Models transferred from GPU to FPGA retained an F1 score of 91.3%, compared to 93.6% when trained directly on the FPGA dataset. This small drop indicates robust generalization. However, the ASIC→SoC transfer resulted in a slightly larger F1 decline, reinforcing that transferability is highly dependent on domain alignment. These results support the notion that CDTL is highly effective when architectural domains share operational semantics, while additional tuning or hybrid models are needed for structurally divergent domains.

6. Conclusion and Future Work

This study confirms the potential of cross-domain transfer learning to accelerate validation processes in heterogeneous computing systems. While results are promising, limitations exist in cases of extreme domain divergence. Future work will focus on automated feature adaptation, hybrid training pipelines, and integration with formal verification.

We also plan to release a benchmark suite for CDTL validation tasks across popular architectures to facilitate reproducibility and future research.

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