Journal of Engineering Science and Technology
Vol. 13, No. 11 (2018) 3619 - 3631

PERFORMANCE AND A NEW 2-D ANALYTICAL MODELING OF A DUAL-HALO DUAL-DIELECTRIC TRIPLE-MATERIAL SURROUNDING-GATE-ALL-AROUND (DH-DD-TM-SGAA) MOSFET

NEERAJ GUPTA*, JANAK KUMAR B. PATEL, ASHOK KUMAR RAGHAV

Amity School of Engineering and Technology, Amity University, Haryana
*Corresponding Author: neerajsingla007@gmail.com

Abstract

This proposed work covers the effect of dual halo structure with dual dielectric. A 2-D analytical model for potential distribution, threshold voltage, electric field and sub-threshold swing has been described through the Poisson's equation solution for a novel structure known as dual-halo dual-dielectric triple-material surrounding-gate MOSFET to diminish short channel effects. The new device has been incorporated with Dual halo near the source and drain sides, while the electrode at the gate incorporates three dissimilar work function metals. A relative estimation of short channel effects (SCEs) for DH-DD-TM-SG, triple-material surrounding-gate (TM-SG) and single-halo triple-material surrounding-gate (SH-TM-SG) MOSFETs has also been carried out in terms of threshold-voltage-roll-off, drain induced barrier lowering, hot carrier effects, and also sub-threshold swing. The proposed novel structure significantly reduces the SCEs. Therefore, DH-DD-TM-SG MOSFETs have superior performance than TM-SG and SH-TM-SG MOSFETs. The efficiency of the Dual halo-doped device is investigated. The proposed model demonstrates its validity by a comparing the simulated results from already published devices obtained by using TCAD Silvaco.

Keywords: Dual dielectric structure, Halo implant, SCEs, Surrounding gate; Triple metal.

1. Introduction

Today's VLSI era requires high performance, high speed, low power and small dimension devices. Scaling down of conventional planar MOSFET leads to unpredictable behaviour, which is known as short channel effects (SCEs). These effects incorporate drain induced barrier lowering (DIBL), sub-threshold swing, roll off of threshold voltage, hot carrier effects and degradation in current driving capacity. These SCEs become an obstacle for further downscaling while establishing a good performance. The vigorous electric field close to drain side induces the hot carrier effect. The DIBL occurs due to increase in the voltage adjacent to drain side, which causes the channel to become more inviting towards the electrons, and the potential barrier is lowered. The multigate transistor including double, triple and cylindrical gates surrounding MOSFET appear to be possible solutions to SCEs. Among all of these cylindrical surrounding gates

MOSFET offers high performance and packaging density. In SG MOSFET, channel is completely surrounded by the gates to provide better control and increase the current driving capability and also enhance the immunity against short channel effects. Therefore, SG MOSFET is a potential option over the conventional MOSFET.

Currently, diverse gate engineering structures have been examined [1]. One such device structure such as the Triple material gate has been investigated. In this TMG structure, three dissimilar metal gate electrodes are utilized with disparate work function. This disparity produces a step potential profile and a crest field in the channel. It boosts up the carrier transportation efficiency and therefore, overcome the SCEs. As presented by Sharma et al. [2] and Pravin et al. [3], in lieu of SiO_2, high dielectric constant oxide as gate insulators is used to inhibit the direct tunnelling leakage current, which arises due to the downscaling of device dimensions.

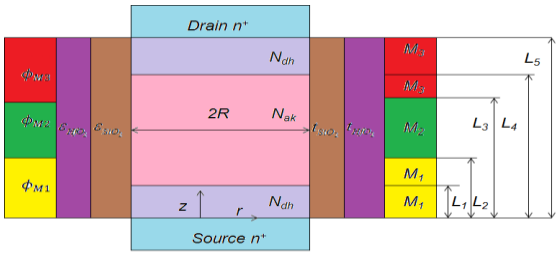
The study shows that superseding of oxide layer with attached high K dielectric decreases the performance of the MOSFET device and the gate electrode control over the channel. So a narrow interfacial oxide layer is used along with high K dielectrics to decrease the density of interface trap charge. Therefore, it minimizes the gate-leakage and increases the electric field inside the channel. Thus, it improves carrier transportation efficiency [4]. The analytical model for DH-DD-TM-SG MOSFET has been developed, which is more beneficial than SH-TM-SG and TM-SG MOSFETs. The roll-off of the threshold voltage is ones of the major problems that happen in nanosize MOSFET devices. According to Sarkar et al. [5], the incorporating halo implant further minimizes the device. Hence, the SCEs can be further minimized by proposed novel structure, which amalgamates the benefits of TM-SG MOSFET and halo. This is also called as DH-DD-TM-CGAA MOSFET. The potential and the field in the channel have been demonstrated by 2-D analytical model. The result shows that DH-DD-TM-SG improves short channel immunity and transport efficacy with respect to SH-TM-SG MOSFET. The analytical results have been examined vis-à-is the simulated results using device simulator ATLAS 3D to validate the model [6].

2. Model Description

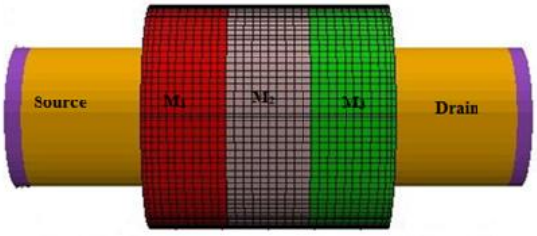
Figure 1 shows the schematic diagram of DH-DD-TM-SG MOSFET structure. Figure 1(a) shows that the gate terminal consists of three metals with different work functions for surrounding gate MOSFET [7]. The gate material 1 with the work function Φm_1=4.8 ev (Au), gate material 2 with Φm_2=4.6 ev (Mo) and gate material

3 with Φm_3=4.4 ev (Ti) respectively. In this Triple metal gate schematic, the symmetric dual halo doping is *incorporated* for the first time along with dual dielectric to form a novel device structure. The channel lengths as shown in Fig. 1(a), under the gate materials are L_2, L_3-L_2 and L_5-L_3 respectively. The lengths L_1 and L_5-L_4 are halo doped with concentration N_{dh}, while the rest of the regions are doped with acceptor doping concentration N_{ak}, assuming that N_{dh} is greater than N_{ak} [8, 9].

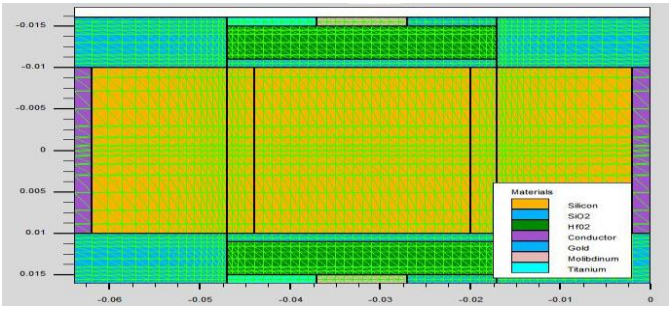
It may be noted from the figure that the metal gate electrode work function (Φm_1) at channel length L_2 is more than the metal gate electrode work function (Φm_3) at channel length L_5-L_3. The metal gate (Φm_1) at the source side is known as a control gate whereas metal gate (Φm_3) at the drain side is known as screen gate. Based on a study by Padmanaban et al. [10], the t_{Sio2}=1 nm and t_{HfO2}=4 nm is the thicknesses of the inner and outer oxide layers respectively. The length of channel region and the diameter of the device is more than 30nm and 10 mm respectively. So, for the recent analysis, quantum effects are ignored [11]. The simulated structure of the proposed device used in the TCAD Silvaco is depicted in Fig. 1(b). The ATLAS simulated mesh profile of the DH-DD-TM-SG MOSFET design is shown in Fig. 1(c).



(a) Cross sectional schematic of dual-halo dual-dielectric triple-material surrounding-gate MOSFET.



(b) Simulated structure of the proposed device used in the analysis.



(c) ATLAS simulated mesh profile of DH-DD-TM-SG MOSFET.
Fig. 1. Dual-halo dual-dielectric triple-material surrounding-gate MOSFET.

3. Mathematical Modelling

The cylindrical coordinate system comprises of a radial direction *r*, an angular component θ in the plane of radial direction, and a vertical direction *z*, as mentioned in Fig. 1(a). The symmetry of the device ensures that surface potential and the field varies with r and z, but not with θ. So 2-D analysis is needed.

The influence of the charge carriers and fixed charges on the electrostatic behaviour of the channel could be avoided. The potential distribution in the channel can be expressed by the Poisson's equation and can be written as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\left[\phi_k(r,z)\right]}{\partial r}\right)+\frac{\partial^2\left[\phi_k(r,z)\right]}{\partial z^2}=\frac{qN_{ak}}{\varepsilon_{Si}}\quad(L_{k-1}\le z\le L_k) \tag{1}$$

where k =1, 2, 3, 4, 5, and $N_{a1} = N_{a5} = N_{dh}$, $N_{a2} = N_{a3} = N_{a4} = N_{ak}$.

The potential distribution is approximated using the parabolic profile for DH-DD-TM-CGAA MOSFET in the radial direction and is given by [12].

$$\phi(r,z)=\zeta_0(z)+\zeta_1(z)\,\mathrm{r}+\zeta_2(z)\,\mathrm{r}^2 \tag{2}$$

where the constant $\zeta_0(z)$, $\zeta_1(z)$ and $\zeta_2(z)$ can be attained by substituting conditions at the boundary.

For obtaining surface potential, the corresponding boundary conditions are:

(1) Surface potential $\phi_s(z)$ depends on *z* only

$$\phi(\mathrm{R},z)=\phi_s(z) \tag{3}$$

(2) The centre potential $\phi_c(z)$ depends on z only

$$\phi(0,z)=\phi_c(z)=\zeta_0(z) \tag{4}$$

(3) The metal gates have a continuous electric flux at the interfaces of the gates/oxide. Therefore,

$$\left.\frac{d\phi_k(r,z)}{dr}\right|_{r=R}=\frac{C_{oxeffdh}}{\varepsilon_{Si}}(\mathrm{v}_{gs}-\phi_{sk}(z)-\mathrm{v}_{fbk})=2R\zeta_2(z) \tag{5}$$

where k =1, 2, 3, 4 and $C_{oxeffdh}$ is the effective gate oxide capacitance for DH-DD-TM-SG MOSFET [13].

$$C_{oxeffdh}=\frac{\varepsilon_{SiO_2}}{R\ln\left[1+\dfrac{t_{oxeffdh}}{R}\right]} \tag{6}$$

where $t_{oxeffdh}$ is the effective gate oxide thickness for DH-DD-TM-SG MOSFET [14].

$$t_{oxeffdh}=t_{SiO_2}+\frac{\varepsilon_{SiO_2}}{\varepsilon_{HfO_2}}t_{HfO_2} \tag{7}$$

Using the boundary conditions, Eqs. (3)-(7), in the surface potential equation, Eq. (2) and then substituting in Eq. (1).

Surface potential is expressed as

$$\frac{d^2\phi_s(z)}{dz^2} - \phi_s(z)\left(\frac{2C_{oxeffdh}}{\varepsilon_{Si}R}\right) + (\mathrm{v}_{gs} - \mathrm{v}_{fbk})\left(\frac{2C_{oxeffdh}}{\varepsilon_{Si}R}\right) = \frac{qN_{ak}}{\varepsilon_{Si}} \tag{8}$$

$$\frac{d^2\phi_s(z)}{dz^2} - \kappa^2\phi_s(z) = \chi \tag{9}$$

where $\kappa^2 = \dfrac{2C_{oxeffdh}}{\varepsilon_{Si}R}$

$$\chi = \frac{qN_{ak}}{\varepsilon_{Si}} - \kappa^2(\mathrm{v}_{gs} - \mathrm{v}_{fbk})$$

Surface potential for all five regions are given as

$$\frac{d^2\phi_{sk}(z)}{dz^2} - \kappa^2\phi_{sk}(z) = \chi_k \qquad l_{k-1} \le z \le l_k \tag{10}$$

$$\chi_k = \frac{qN_{ak}}{\varepsilon_{Si}} - \kappa^2(\mathrm{v}_{gs} - \mathrm{v}_{fbk}) \tag{11}$$

where k =1, 2, 3, 4, 5

$$\mathrm{v}_{fbj} = \phi_{mj} - \left\{\chi_s + E_g - q\phi_{fp}\right\} \tag{12}$$

where j = 1, 2, 3, 4, 5

$$\phi_{fp} = \frac{KT}{q}\ln\left(\frac{N_{ak}}{n_i}\right) \tag{13}$$

The solution of second order differential equation, Eq. (10), through the complementary and the particular integral functions is given as

$$\phi_{si}(z) = \alpha_k e^{(\kappa z)} + \beta_k e^{(-\kappa z)} - \frac{\chi_k}{\kappa^2} \qquad l_{k-1} \le z \le l_k$$

$$M_k = \frac{\chi_k}{\kappa^2} \tag{14}$$

$$\delta_k = \exp(\kappa L_k)$$

$$\delta_k^{-1} = \exp(-\kappa L_k)$$

where $_k$ and β_k are arbitrary constants, which are calculated with the help of continuity conditions for the surface potential distribution (ϕ) and the field distribution (E) at the interfaces of different metal gates [8, 9]. The value of α_k and β_k reported in literature [15].

(1) The potential ϕ_{s1}, at the source end is given by

$$\phi_{s1}(z)\big|_{z=0} = V_{b1} \tag{15}$$

$$V_{b1} = \frac{KT}{q}\ln\left(\frac{N_{a1}N_d}{n_i^{\,2}}\right) \tag{16}$$

(2) The potential ϕ_{s5}, at the drain end is given by

$$\phi_{s5}(z)\big|_{z=l} = V_{b5} + V_{ds} \tag{17}$$

$$V_{b5} = \frac{KT}{q}\ln\left(\frac{N_{a5}N_d}{n_i^{\,2}}\right) \tag{18}$$

(3) The surface potential ϕ is continuous functions at the interfaces of different metal gates and can be written as

$$\phi_{sk}(z)\big|_{z=l_k} = \phi_{s(k+1)}(z)\big|_{z=l_k} \tag{19}$$

where k =1, 2, 3, and 4

(4) The electric fields E is continuous functions at the interfaces of dissimilar metal gates and can be written as

$$\left.\frac{d\left[\phi_{sk}(z)\right]}{dz}\right|_{z=l_k} = \left.\frac{d\left[\phi_{s(k+1)}(z)\right]}{dz}\right|_{z=l_k} \tag{20}$$

where k =1, 2, 3, and 4.

The electric field distribution is obtained by differentiating surface potential with respect to radial direction z.

$$E_{\mathrm{k}(z)} = -\frac{d\phi_{sk}(z)}{dz} = \kappa(\beta_k e^{(-\kappa z)} - \alpha_k e^{(\kappa z)}) \tag{21}$$

The halo part indicating higher work function in metal gates, determines the minimum surface potential for the DH-DD-TM-CGAA MOSFET.

Differentiating surface potential equation, Eq. (14), relative to the direction z and making it zero for getting the minimum surface potential $\phi_{s1\min}$.

$$\left.\frac{d\phi_{s1}(z)}{dz}\right|_{Z_{\min}} = 0 \quad z_{\min} = \frac{1}{2\kappa}\ln\frac{\beta_1}{\alpha_1},$$

$$\phi_{s1\min} = 2\sqrt{\alpha_1\beta_1} - \frac{\chi_1}{\kappa^2} \tag{22}$$

As explained by Wang et al. [16], the device turn ON voltage is threshold voltage, which is twice the Fermi potential and equal to minimum surface potential.

$$\phi_{s1\min} = 2\phi_f$$

$$2\sqrt{\alpha_1\beta_1}-\frac{\chi_1}{\kappa^2}=2\frac{KT}{q}\ln\left(\frac{N_{ak}}{n_i}\right)\Bigg|_{v_{gs}=v_{th}} \tag{23}$$

Sub-threshold swing is given by [17, 18].

$$SS_{dh}=2.303\frac{KT}{q}\frac{1}{\frac{d\phi_{s1\min}}{dv_{gs}}} \tag{24}$$

4. Results and Discussion

The present analysis is carried out for surface potential ϕ_s, electric field E, threshold voltage v_{th}, sub-threshold swing S, drain induced barrier lowering and roll off of threshold voltage [19]. Simulation parameters are: V_{gs}=0.2 V, V_{ds}=0.1 V, R=10 nm, $t_{oxeffdh}$ =1.78 nm, N_{dh}=10^{24} m^{-3}, N_{ak}=10^{23} m^{-3}, N_d=10^{26} m^{-3}, L=30 nm. The dielectric constants of silicon and hafnium oxide are 3.9 and 20 respectively. The surface potential of DH-DD-TM-SG, SH-TM-SG and TM-SG MOSFET structure is plotted in Fig. 2.

Figure 2 shows that triple material structure has two step function profile, which is a clear indication of a reduction in SCEs. These gradual steps function profile at the interface screens the higher metal gate M_1 work function region from the fluctuation of drain potential. Enhanced V_{ds} is discarded across the lower metal gate M_3 work function region. It is noticed that the minimum surface potential ϕ_s happens for DH-DD-TM-SG MOSFET in the halo region as compared to SH-TM-SG and TM-SG MOSFET. In this novel device, there are additional steps at the drain and source sides. Normally there are three step function profiles in SH-TM-SG but for Dual halo, it is realized that the surface potential of DH-DD-TM-SG exhibits four step function profiles. Therefore, this extra step profile further helps in scale down the short channel influence and improving the current driving capability. The analytical results are well collaborating with simulated results validating the model.

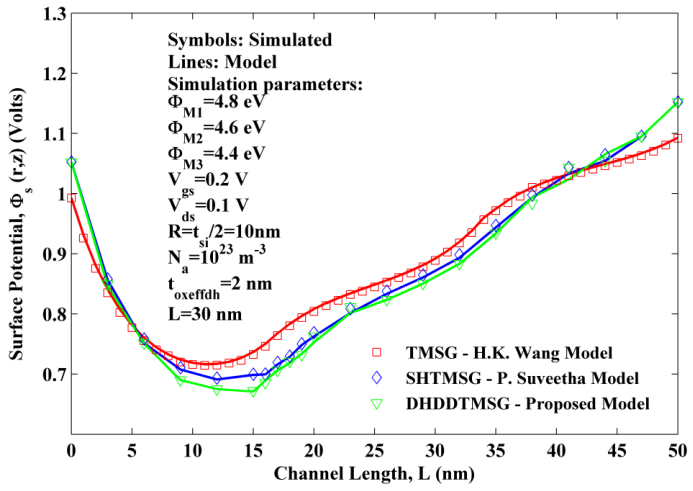


Fig. 2. Graph of the surface potential with variation in channel length.

Figure 3 depicts the variation of minimum surface potential ϕ_{s1min} as a function of the channel length for R=10 nm

It is observed that Dual halo structures having lowered minimum surface potential as their counterpart SH-TM-SG and TM-SG structures which outcomes in raised the device efficiency. The simulated results agree with the analytical results validating the model.

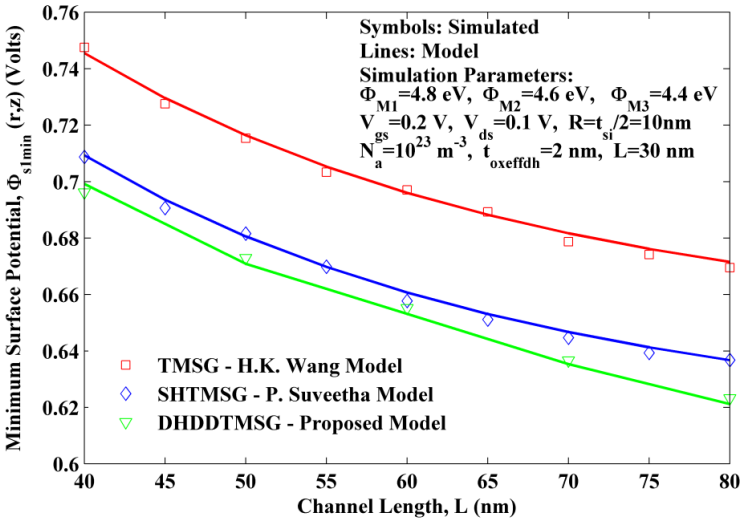


Fig. 3. Graph for the minimum surface potential distribution with varying channel length for all the three devices.

Figure 4 shows the electric field distribution of DH-DD-TM-SG, SH-TM-SG and TM-SG MOSFET structure. The drain side having lower metal gate M_3 work function region points to a valuable diminution in electric field. The carriers in the channel region experience fall in the electric field near to drain region, which causes reduction in HCEs. Therefore, it improves the overall transport efficiency. From Fig. 4, it can be seen that an additional peak of field is observed over the halo barrier, which further enhances the characteristics of the novel device. In contrary to Single halo structure, there are more peaks in Dual halo structure, thereby improving immunity against SCEs. The further increment in halo doping concentration reforms the beginning peak. The second peak of the gate metal improves with further rise in work function. Hence speeds up the carriers in the channel. The analytical results are close to simulated results which validates the model.

DH-DD-TM-SG has a less threshold voltage [20] in comparison to Single halo and TM-SG MOSFETs devices owing to improved gate controllability, Fig. 5. The percentage difference in threshold voltage in the proposed model and TM-SG [16] is 23% at channel length 20 nm. The percentage difference in threshold voltage in the proposed model and SH-TM-SG [8] is 17% at channel length 20 nm. Thus, the DH-DD-TM-SG is suitable for low voltage applications.

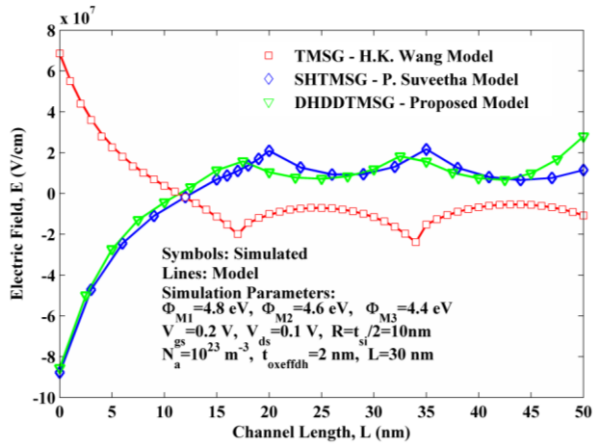


Fig. 4. Electric field distribution with varying channel length for TM-SG, SH-TM-SG and DH-DD-TM-SG devices.

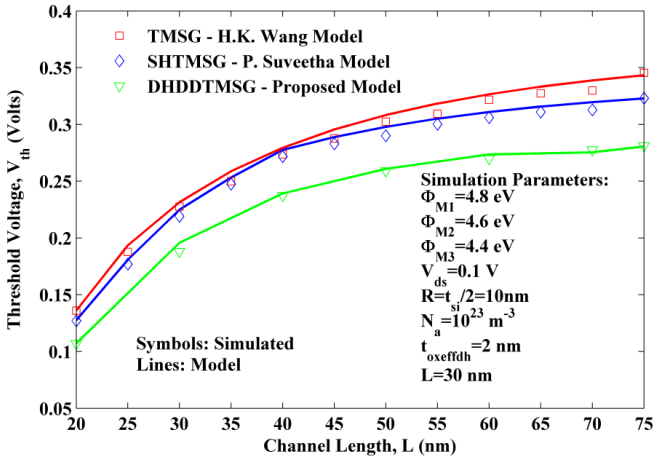


Fig. 5. Threshold voltage variation with channel length for different devices.

Figure 6 illustrates the variation of sub-threshold swing with channel length for DH-DD-TM-SG, SH-TM-SG and TM-SG MOSFET structure. The incorporation of Dual halo structure along with dual dielectric for triple material gate shows reduction in sub-threshold swing for DH-DD-TM-SG in comparison to SH-TM-SG and TM-SG MOSFET devices, exhibiting immunity against SCEs. However, there is not much significant difference for the channel length above 80 nm [21, 22].

DIBL is a short channel effect that comes into picture after application of large drain bias and adversely affecting the device performance. The barrier between the source and the channel is reduced and hence gate has a limited control over the channel [23, 24].

Figure 7 gives the variation of DIBL with the channel length for DH-DD-TM-SG, SH-TM-SG and TM-SG MOSFET devices. It is clear from Fig. 7 that DH-DD-TM-SG has a very low value of DIBL as compared to SH-TM-SG device. Hence,

it shows that the dual halo structure in DH-DD-TM-SG MOSFET leads to suppression of SCEs. The analytical results are well collaborating with simulated results validating the model.

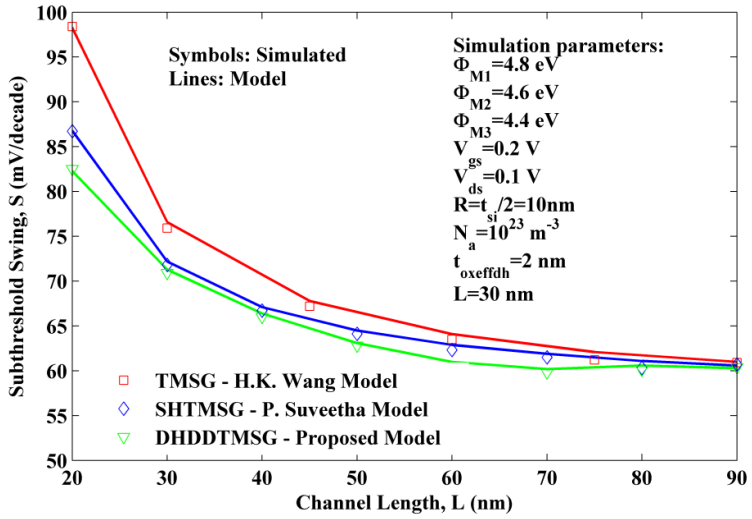


Fig. 6. Variation in sub-threshold swing as a function of the channel length.

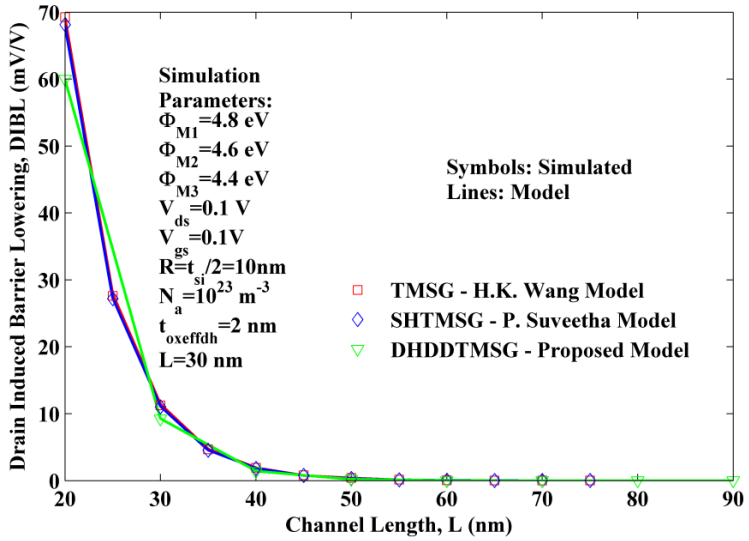


Fig. 7. Graph of drain induced barrier lowering with varying channel length.

As presented by Pradhan et al. [25] and Dasgupta et al. [26], the diminution of threshold voltage with diminution in gate length is a well-known SCE called the "V_t-roll off". Figure 8 shows the plot of the roll-off of threshold voltage for DH-DD-TM-SG, SH-TM-SG and TM-SG MOSFET with position along the channel. The roll-off of threshold voltage has been determined by evaluating the difference between the threshold voltages for shorter channel and for long channel length devices. Figure 8 depicts that the increase in gate length increases the V_t-roll off. The analytical model of V_t-roll off is plotted in Fig. 8 and has been verified by using TCAD Silvaco.

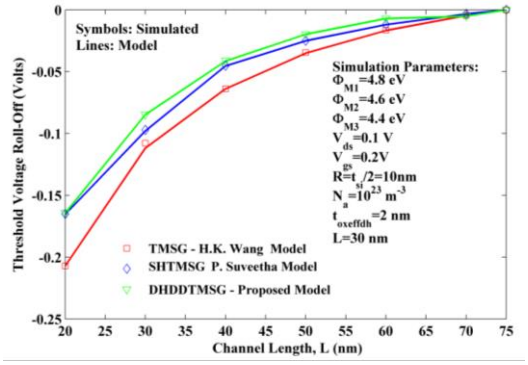


Fig. 8. Threshold voltage roll-off versus the variation in channel length.

5. Conclusions

In this paper, a 2-D analytical model for the novel device DH-DD-TM-SG MOSFET has been developed by using a parabolic approximation. Using gate engineering structure along with halo implant shows further improvement in minimization of SCEs. An additional peak is induced in the electric field profile, which describes the reduction in hot carrier effects. The reduction in sub-threshold swing, roll-off of threshold voltage and drain induced barrier lowering are the direct result of halo and gate engineering structures. Thus, it is manifest that the combination of triple metal gates along with dual dielectric and halo implant architecture leads to further enhance in short channel behaviour. Thus, it further ensures improvement in the carrier transport efficiency. The DH-DD-TM-SG MOSFET shows superior performance over TM-SG and SH-TM-SG devices for lowering HCEs and SCEs.

Nomenclatures

$C_{oxeffdh}$	Oxide capacitance, F
E_g	Energy band gap, eV
N_{ak}	Acceptor ion concentration, atoms/m^3
Q	Electronic charge
R	Radius of silicon pillar, nm
$t_{oxeffdh}$	Oxide thickness, nm
V_{fbk}	Flat-band voltage, V

Greek Symbols

ε_{Si}	Permittivity of silicon
ϕ_{fp}	Fermi potential, eV
$\phi_k(r,z)$	Surface potential, V
ϕ_{mk}	Work function of metal, eV
χ_s	Electron affinity, eV

Abbreviations

TM-SG	Triple Material Surrounding Gate

References

1. Long, W.; Ou, H.; Kuo, J.-M.; and Chin, K.K. (1999). Dual material gate field effect transistor. *IEEE Transactions on Electron Devices*, 46(5), 865-870.
2. Sharma, A.; Jain, A.; Pratap, Y.; and Gupta, R.S. (2016). Effect of high K and vacuum dielectrics as gate stack on junctionless cylindrical surrounding gate MOSFET. *Solid State Electronics*, 123, 26-32.
3. Pravin, J.C.; Nirmal, D.; Prajoon, P.; and Ajayan, J. (2016). Implementation of nanoscale circuits using dual metal gate engineered nanowire MOSFET with high-k dielectrics for low power applications. *Physica E: Low Dimensional Systems and Nanostructures*, 83, 95-100.
4. Ghosh, P.; Haldar, S.; Gupta, R.S.; and Gupta, M. (2012). Analytical modeling and simulation for dual metal gate stack architecture (DMGSA) cylindrical/surrounded gate MOSFET. *Journal of Semiconductor Technology and Science*, 12(4), 458-466.
5. Sarkar, A.; De, S.; and Sarkar, C.K. (2012). Asymmetric halo and symmetric single halo dual material gate and double halo dual material gate n-MOSFETs characteristic parameter modelling. *International Journal of Numerical Modelling Electronic Networks, Devices and Fields*, 26(1), 41-55.
6. Silvaco International. (2004). Atlas user's manual: Device simulation software, Santa Clara, California.
7. Dubey, S.; Santra, A.; Saramekala, G.; Kumar, M.; and Tiwari, P.K. (2013). An analytical threshold voltage model for triple-material cylindrical gate-all-around (TM-CGAA) MOSFETs. *IEEE Transactions on Nanotechnology*, 12(5), 766-774.
8. Dhanaselvam, P.S.; Balamurugan, N.B.; Chakaravarthi, G.C.V.; Ramesh, R.P.; and Kumar, B.R.S. (2014). A 2D analytical modeling of single halo triple material surrounding gate MOSFET. *Journal of Electrical Engineering & Technology*, 9(4), 1355-1359.
9. Dhanaselvam, P.S.; and Balamurugan, N.B. (2014). A 2D sub-threshold current model for single halo triple material surrounding gate MOSFETs. *Microelectronics Journal*, 45(6), 574-577.
10. Padmanaban, B.; Ramesh, R.; Nirmal, D.; and Sathiyamoorthy, M.S. (2015). Numerical modeling of triple material gate stack gate all around (TMGSGAA) MOSFET considering quantum mechanical effects. *Superlattices and Microstructures*, 82, 40-54.
11. Naveh, Y.; and Likharev, K.K. (2000). Modeling of 10-nm-scale ballistic MOSFET's. *IEEE Electron Device Letters*, 21(5), 242-244.
12. Young, K. K. (1989). Short channel effect in fully depleted SOI MOSFETs. *IEEE Transactions on Electron Devices*, 36(2), 399-402.
13. Jimenez, D.; Iniguez, B.; Sune, J.; Marsal, L.F.; Pallares, J.; Roig, J.; and Flores, D. (2004). Continuous analytic I-V model for surrounding gate MOSFETs. *IEEE Electron Device Letters*, 25(8), 571-573.
14. Cheng, B.; Cao, M.; Voode, P.V.; Greene, W.; Stork, H.; Yu, Z.; and Woo, J.C.S. (1999). Design considerations of high-K gate dielectrics for sub-0.1-μm MOSFET's. *Proceedings of the 28th European Solid-State Device Research Conference*. Bordeaux, France, 308-311.

15. Gupta, N.; Patel, J.K.B.; and Raghav, A.K. (2018). Modeling and analysis of threshold voltage for dual-halo dual-dielectric triple-material surrounding-gate metal-oxide-semiconductor field-effect transistors. *International Journal of Pure and Applied Mathematics*, 118(18), 3759-3771.
16. Wang, H.-K.; Wu, S.; Chiang, T.-K.; and Lee, M.-S. (2012). A new two-dimensional analytical threshold voltage model for short-channel triple-material surrounding-gate metal-oxide-semiconductor field-effect transistors. *Japanese Journal of Applied Physics*, 51(5R).
17. Tiwari, P.K.; Dubey, S.; Singh, K.; and Jit, S. (2012). Analytical modeling of subthreshold current and subthreshold swing of short-channel triplematerial doublegate (TM-DG) MOSFETs. *Superlattices and Microstructures*, 51(5), 715-724.
18. Rewari, S.; Haldar, S.; Nath, V.; Deswal, S.S.; and Gupta, R.S. (2015). Numerical modeling of subthreshold region of junctionless double surrounding gate MOSFET. *Superlattices and Microstructures*, 90, 8-19.
19. Verma, J.H.K.; Haldar, S.; Gupta, R.S.; and Gupta, M. (2015). Modeling and simulation of subthreshold behaviour of cylindrical surrounding double gate MOSFET for enhanced electrostatic integrity. *Superlattices and Microstructures*, 88, 354-364.
20. Dutta, T.; Pahwa, G.; Agarwal, A.; and Chauhan, Y.S. (2018). Impact of process variations on negative capacitance FinFet devices and circuits. *IEEE Electron Device Letters*, 39(1), 147-150.
21. Gola, D.; Singh, B.; and Tiwari, P.K. (2017). A threshold voltage model of tri-gate junctionless field effect transistors including substrate bias effects. *IEEE Transactions on Electron Devices*, 64(9), 3534-3540.
22. Kumar, A.; Bhushan, S.; and Tiwari, P.K. (2017). Analytical modeling of subthreshold characteristics of ultra-thin double gate-all-around (DGAA) MOSFETs incorporating quantum confinement effects. *Superlattices and Microstructures*, 109, 567-578.
23. Xiao, Y.; Zhang, B.; Lou, H.; Zhang, L.; and Lin, X. (2016). A compact model of subthreshold current with source/drain depletion effect for the short-channel junctionless cylindrical surrounding-gate MOSFETs. *IEEE Transactions on Electron Devices*, 63(5), 2176-2181.
24. Rawat, A.S.; and Gupta, S.K. (2017). Potential modeling and performance analysis of junctionless quadruple gate MOSFET for analog and RF applications. *Microelectronics Journal*, 66, 89-102.
25. Pradhan, K.P.; Kumar, M.R.; Mohapatra, S.K.; and Sahu, P.K. (2015). Analytical modeling of threshold voltage for cylindrical gate all around (CGAA) MOSFET using center potential. *Ain Shams Engineering Journal*, 6(4), 1171-1177.
26. Dasgupta, A.; Rastogi, P.; Agarwal, A.; Hu, C.; and Chauhan, Y.S. (2018). Compact modelling of cross-sectional scaling in gate-all-around FETs: 3-D to 1-D transitions. *IEEE Transactions on Electron Devices*, 65(3), 1094-1100.