DESIGN CHARGE-PUMP PHASE-LOCKED LOOP (CPPLL) USING 0.35µm VLSI TECHNOLOGY

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Abstract : ***CMOS refer a particular design of digital circuitry design, and that circuit to integrated circuit (chip) of the family process used for implementation. In this paper, we use 0.35µm VLSI technology and compare the power dissipation of CPPLL with the different blocks. PFD (Phase Frequency Detector), Charge Pump, Loop Filter, VCO (Voltage Controlled Oscillator), Frequency Divider. In today's wireless communication system, greater maximum frequency required by the CPPLL with respect to the digital phones that use these circuit law, power consumption, small size and cost is important design factor of low fabrication. In this paper we take each of these component and design, simulate them using various combination we work to improve the efficiency of the system.***

IndexTerms - Design Charge-Pump Phase-Locked Loop, TSMC 0.35µm, Power Optimization, CMOS Logic.

I. INTRODUCTION

A charge-pump phase-locked loop is a control system that generates an output signal whose phase is related to the phase of an input signal. While there are several different types, it is easy to initially visualize as an electronic circuit consisting of a detector. The oscillator generates a periodic signal. The phase detector compares the phase of that signal with the phase of the input periodic signal and adjusts the oscillator to keep the phase matched. Phase-locked loop are widely used employed in radio, telecommunication, computers and other electronic application. They can be used to demodulate a signal, recover a signal from a noisy communication channel, and generate a stable frequency at multiples of an input frequency (frequency synthesis).

A typical implementation of the CPPLL consists of a phase frequency detector (PFD), a CP, a passive loop filter (LF), and a voltage controlled oscillator (VCO). The CPPLL system is shown in Figure 1. A divider is used in feedback, in applications requiring clock multiplication but is omitted here for simplicity. The PFD commonly generates a pair of digital pulses corresponding to the phase/frequency error between the reference clock and the VCO output by comparing the positive (or negative) edges of the two inputs. The CP then converts the digital pulses into an analog current that is converted to a voltage via the passive loop network. The resulting control voltage drives the VCO. The negative feedback loop forces the phase/frequency error to zero. Like any other feedback system, a CPPLL has to be designed with a proper consideration for stability.

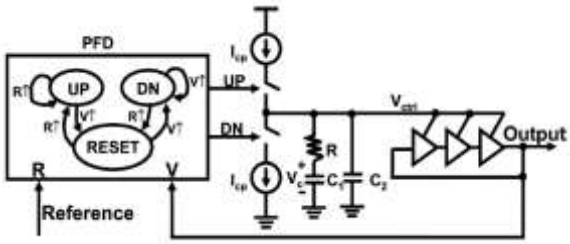

Figure 1: Third-order CPPLL Block Diagram[1]

II. RELATED WORK

CHARGE-PUMP PHASE-LOCKED LOOP (CPPLL) is widely used as clock generators in a variety of applications including microprocessors, wireless receivers, serial link transceivers, and disk drive electronics. One of the main reasons for the widely adopted use of the CPPLL in most PLL systems is because it provides the theoretical zero static phase offset, and arguably one of the simplest and most effective design platforms. The CPPLL also provides flexible design tradeoffs by decoupling various design parameters such as the loop bandwidth, damping factor, and lock range. While there are numerous CPPLL design examples in the literature, precise analysis and a mathematical clarity of the loop dynamics of the CPPLL is lacking. The two most popular references in this arena by Hein and Scott [1], and Gardner [2], provide useful insight and analysis PLLs. Several other references [3], [4], provide simplified yet useful approximations of third-order CPLLs. However, they do not provide a complete and extensive analysis for practical integrated circuit (IC) PLLs, i.e., third-order CPLLs.

Charge-pump phase-locked loop are widely used in electronics components and synchronization purposes, in space communication for coherent demodulation and threshold extension, bit synchronization, and symbol synchronization. Charge-pump phase-locked loop can also be used to synthesis new frequencies which are multiple of a reference frequency with the same stability. We utilize charge-pump phase-locked loop as a concrete example. CPPLL is a representative mixed-signal circuit [5].

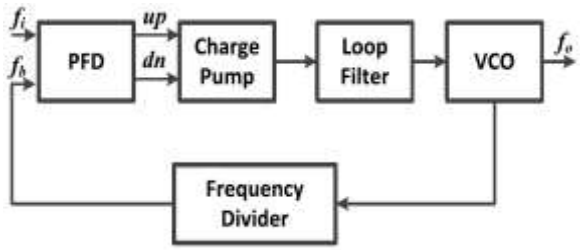

Figure 2: CPPLL Block Diagram[12]

III. PHASE FREQUENCY DETECTOR

A Phase Frequency Detector (PFD), in electronics, is a device which compares the phase of two input signals. It has two inputs which correspond to two different input signals, usually one from a frequency divider and other input from external source. It has two inputs which instruct subsequent circuitry on how to adjust to look into the phase. [6]

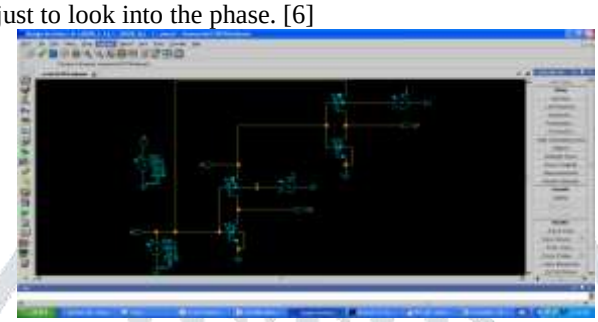

Figure 3: Circuit Diagram of PFD For Simulation

The circuit diagram of proposed PFD is as shown in below Figure 3, it work similar to conventional PFDs but it has many advantages compared to conventional PFDs. This PFDs is basically construct with two GDI (Gate Diffusion Input) cells. A basic GDI cell contains four terminals – G (common gate input of NMOS and PMOS transistor), P (the outer diffusion node of PMOS transistor), N (the outer diffusion node of NMOS transistor), and D (common diffusion node of both transistor). This reducing allow for reducing power consumption, propagation delay, and area of digital circuits.

When Fclk is equal to Fvco both the outputs that is UP and DOWN are zero, if Fclk is high compared to Fvco then UP signal is high else DOWN signal is high indicating the phase error between Fclk and Fvco.

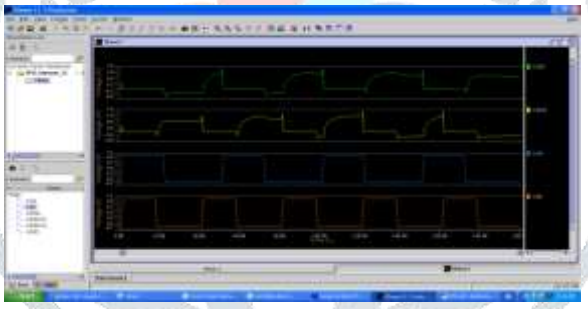

Figure 4: Input and Output Waveform of PFD

IV. CHARGE-PUMP and LOOP FILTER

Charge Pump is the circuit that translates the UP and DOWN signals from the PFD to control voltage that will control the VCO. As shown in Figure 5, charge pump consist of two switched current sources implemented using NMOS and PMOS diode connected load. Charge pump is switched on and off by the PFD output signals UP and DOWN. This charge pump consists of two switched current sources that pump charge into or out of the loop filter according to the PFD output. [7]

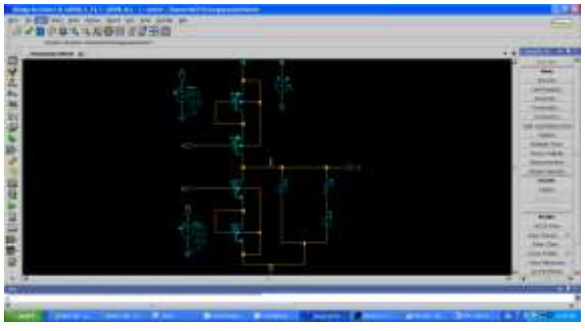

Figure 5: Circuit Diagram of Charge-Pump and Loop Filter

This UP signals from the PFD will turn the UP switch (PMOS) on, and it will cause the CP to inject current into the loop filter, increasing V_{out}. When the feedback leads the reference signal, the PFD detects a rising edge on the feedback signal and will produce a DOWN signal. This DOWN signal from the PFD will turn the DOWN switch (NMOS) ON, and the CP will sink current out of the loop filter

thus, decreasing V_{out}. Fig. 6 shows the complete simulation result of phase detector with charge pump. It shows that the capacitors is charging only when the UP is high, and will be stable if the UP and DOWN both are low and vice versa.

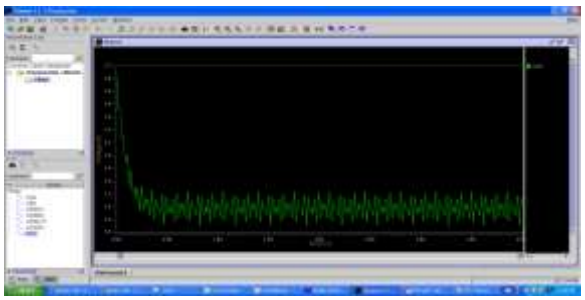

Figure 6: Output Waveform of Charge-Pump and Loop Filter

V. VOLTAGE CONTROLLED OSCILLATOR

We applied the input voltage for determine the instantaneous oscillation frequency. A voltage controlled oscillator using CMOS is work combination of NMOS and PMOS, NMOS and PMOS are connected to each other for simulate of VCO. Input voltage applied then simulate in VCO. A Voltage Controlled Oscillator or VCO is a electronic oscillator whose oscillation frequency due to input voltage. We applied the input voltage for determine the instantaneous oscillation frequency. A voltage controlled oscillator using CMOS is work combination of NMOS and PMOS, NMOS and PMOS are connected to each other for simulate of VCO. Input voltage applied then simulate in VCO.[13]

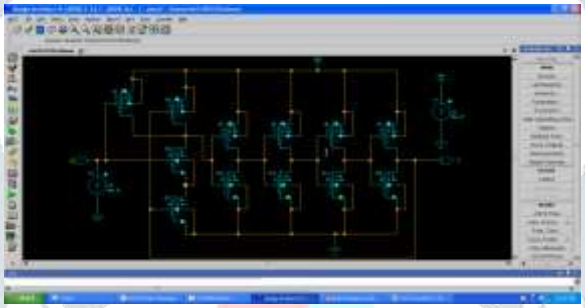

Figure 7: Circuit Diagram of VCO

A ring oscillator is a device work of an odd number of NOT gates. Output oscillates between two voltages, representing 0 or 1. The NOT gates and inverters are connected in series, and output connects the feedback network. If we connected the inverters more than 3 in series, so first inverter replace NAND gates with enable.

An oscillator is an autonomous system which generates a periodic output without any input. The most popular type of the VCO circuit is the current starved voltage controlled oscillator. Here the number of inverter stages is fixed with 5. The simplified view of a single Stage current starved oscillator.

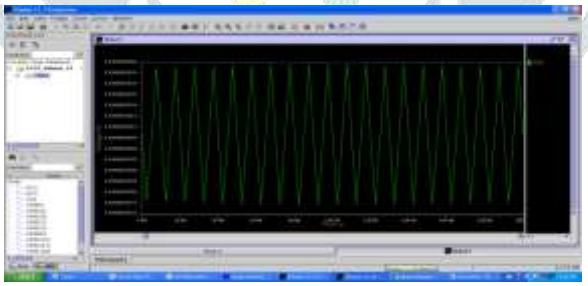

Figure 8: Output Waveform of VCO

VI. FREQUENCY DIVIDER

In modern integrated transceivers operating at microwave frequencies, one of the most critical parts is the frequency divider chain of the PLL frequency synthesizer. The VCO output frequency in the order of several GHz, the problem of actually implement the frequency division at such high frequencies is a non trivial one. Depending on the frequency that also needs to be divided, different approaches can be used.

When the higher frequency division is necessary, a purely analog solution has to be taken into consideration. The two main solutions to multi-GHz frequency division are master-slave latch divider, and injection-locking divider. The master-slave divider employs a two stage regenerative divider based on analog differential latch to perform a divide-by-2 frequency divider stage.

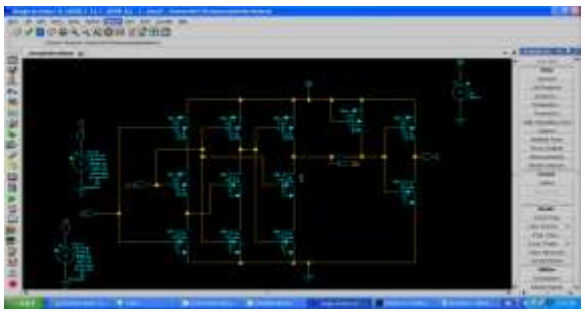

Figure 9: Circuit Diagram of Frequency Divider

A fractional-n frequency synthesizer can be constructed using two integer dividers, a divide-by-n and a divide-by-(n+1) frequency divider. With a modulus controller, n is toggled between the two values so that the VCO alternates between one locked frequency and the other. The VCO stabilizes at a frequency that is the time average of the two locked frequencies.

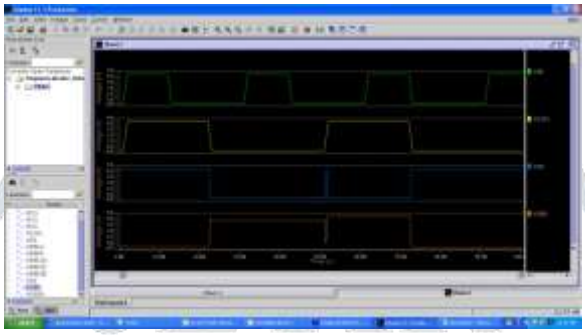

Figure 10: Output Waveform of Frequency Divider

VII. CHARGE-PUMP PHASE-LOCKED LOOP

The phase-locked loop (PLL) is one of the key building blocks in many communication systems; providing a means for maintaining timing integrity and clock synchronization. The PLL can be used in various applications such as timing extraction from data streams, jitter mitigation and frequency synthesis.

We describe the fundamental properties of a charge-pump PLL (CP-PLL). The CP-PLL derives its name from the fact that the phase detector (PD) output is a current source as opposed to a voltage source and "pumps" current into and out of the loop-filter. This form of PLL is popular because it is adaptable to integration in microcircuit devices. Therefore we focus the discussion on methods suitable for ASIC design. We provide mathematical models to study key parameters affecting the loop-bandwidth, peaking, jitter, noise and transient response.

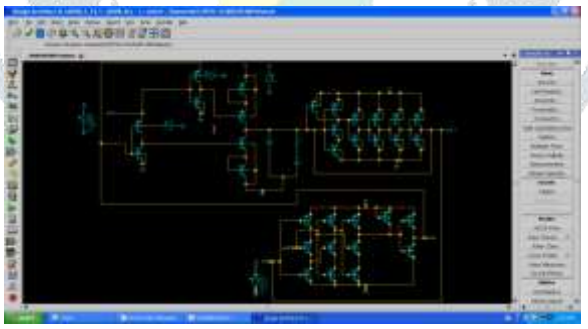

Figure 11: Circuit Diagram of CPPLL

In this circuit diagram, we are doing all components connected to each other. Phase Frequency Detector (PFD), Charge-Pump (CP), Loop Filter, Voltage Controlled Oscillator (VCO) and Frequency Divider for reducing the low power dissipation, high performance, low power supply and low power of CMOS technology.

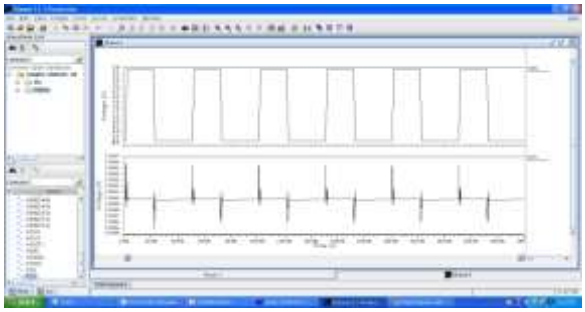

Figure 12: Input and Output Waveform of CPPLL

VIII. CONCLUSION

In this paper we designed CPPLL using 0.35µm CMOS technology. There are all components are implemented using CMOS technology. In this project we use the Charge-Pump for reducing the phase noise of PLL. This CMOS charge-pump structure can be applied in other CPPLL with high performance.

In VCOs we realized 5VCO is better as compared to 7VCO and 9VCO for total power dissipation at all different DC voltages.

In Frequency Divider CMOS devices capabilities for high performance communication circuit. The low supply voltage and low power of CMOS technologies have made them.

A Charge-Pump Phase-Locked Loop (CPPLL) is realized in Mentor Graphics using 0.35µm CMOS technology. The lock time of the CPPLL is less. Which is better than most of the design achieved previously in this process.

REFERENCES

[1] J. Hein and J. Scott, "z-domain model for discrete-time PLLs," *IEEE Trans. Circuits Syst.*, vol. 35, pp. 1393–1400, Nov. 1988.

[2]. F. Gardner, "Charge pump phase-lock loops," *IEEE Trans. Commun.*, vol. COM-28, pp. 1849–1858, Nov 1980.

[3]. I. Novof, J. Austin, R. Kelkar, D. Strayer, and S. Wyatt, "Fully integrated CMOS phase-locked loop with 15 to 240 MHz locking range and _50 ps jitter," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1259–1266, Nov. 1995.

[4]. J. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1723–1732, Nov. 1996.

[5]. Bibhu Prasad Panda, "Department of Electronics and Communication Engineering National Institute of Technology Rourkela

[6]. R. Jacob baker, Harry W. Li and David E. Boyce, "CMOS Circuit Design, Layout and Simulation". IEEE Press series on Microelectronics system, pp. 355-361 and 383-387, 2000

[7]. Tao Xu, Huib Lincklaen Arriëns, Rene van Leuken, Alexander de Graaf, "Department of microelectronics & Computer Engineering, Faculty of Electrical Engineering Mathematics and Computer Science, Delft University of Technology, Netherlands

[8]. Behzad Razavi, "Design of Analog CMOS Integrated Circuit".

[9]. Dr. S.A. Ladhake, "(Sipana's College of Engineering & Technology, Amravati, Maharashtra).

[10]. Ms. Ujwala A. Belorkar, "High Performance Voltage Controlled Oscillator Using 65 NM VLSI Technology" (Hanuman Vyayam Prasa Mandal's College of Engineerig & Technology, Amravati, Maharashtra).

[11]. Pavan Kumar Hanumolu, *Student Member, IEEE*, Merrick Brownlee, *Student Member, IEEE*, Kartikeya Mayaram, *Senior Member, IEEE*, and Un-Ku Moon, *Senior Member, IEEE*

[12]. Liuxi Qian, Zhaori Bi, Dian Zhou, *Senior Member, IEEE*, and Xuan Zeng, *Member, IEEE Trans* Automated Technology Migration Methodology for Mixed-Signal Circuit Based on Multistart Optimization Framework. Vol. 23, No. 11

[13]. Fargab Ahmed, Dr. Janak Kumar Patel and Neeraj Gupta "Voltage Controlled Oscillator (VCO) Using 0.35µm VLSI Technology," Vol. 5 Issue 5, May 2016