ENHANCEMENT OF AN IMAGE BY IMPORTING THE PROPERTIES OF XSG INTO FPGA BOARD

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Abstract*— General outcome of an image that expected the quality and extract its structured information with help of image processing. Time taking to develop the algorithm is more, so we reducing the thousands of lines of code and processing the image application by using xilinx system generator(XSG) to implement into Field Programmable Gate Array(FPGA). This method is generally applied on an image in the literature. Image edges also detected with help of this method. Irrespective of the pixels of image i.e. size of image could be resized and showed enhanced image with all the blocks help could be taken in Matlab/Simulink and xilinx. The concept of basic linear transformation implemented by using Xilinx. The concept of project that exist hardware software co-simulation for processing of an image using Xilinx System Genarator. In this technique that we provide the set of simulink blocks or models for different hardware operations and could be implement on FPGA.This paper proposes as first step towards implement and importing the properties of system generator block into FPGA board(Spartan-6) and produce one block enough to enhanced the given image that leads to processing. The verilog code which helps to do operations efficiently.

***Keywords*—Xilinx System Generator(XSG), Field Programmable Gate Array(FPGA), Matlab, Simulink, Verilog, Spartan-6.**

I.INTRODUCTION

In recent years, the usage of digital images have increased gradually. Everybody wants to get good quality of images from their cameras and keep these images in hard disks for future purpose. We generally want to share or send good quality images via internet, smart phones [1]. The raise in demand of digital images leads to send important documents as in the form of image. There are so many technologies present to enhance the image quality for better appearance for visual and analysis purpose by any machine or human being. Image processing applications like safe driving electric vehicle detection[2].

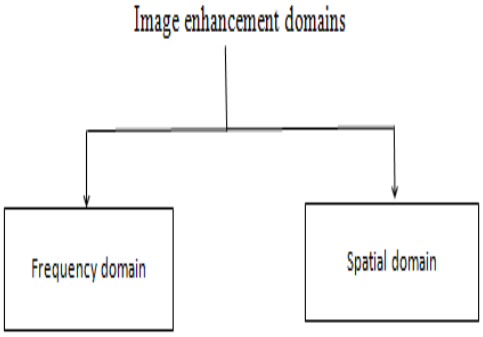
The word image enhancement which implies to distinguish the enhanced image and original image. The appearance of the image in different parts are improving with this enhancement technique. The image that appears very pleasant to see than the original image that used to send.

The processing system of an image could be developed by using FPGA is complex configurable devices that can be implementing logic circuits with equivalent to millions of logic gates. For the high level frame work present in this application based on the well known modeling and simulation tool suite Matlab/Simulink. Here the simulation could be done with help of simulink engine. The rich set blocks that exist in standard libraries of simulink, xilinx blocks which added the advantage of the design of the desired specification which required to execute the project. Especially by designing the basic functionality of the target we use xilinx blocks and that implemented into simulink.

The VLSI/VHDL code which helps to reduce the complexity of the system functionality for the most analysis required part in the project. It explains how the value of the threshold could be decreased and obtain the original desire of the project i.e. piecewise linear transformation function. As we know the HDL which the language explains the how data flow occurs in the given architecture or design. In digital electronics area the FPGA technology brings more attention to develop the image processing applications. It has the advantage of time to market, cost effective, gives rapid prototyping of complex algorithms and reduce the complexity in debugging and verification. FPGA is the perfect choice of implementing image processing algorithms in real time. The processing system of an image could be developed by using FPGA is complex configurable devices that can be implementing logic circuits with equivalent to millions of logic gates.

The proposed system here it reduces the overall complexity in design and helps to enhance the quality of image using FPGA board.

Image enhancement : The perfect observation of an image takes place the increasing quality of an image by human observer. Here it occurs with enhancement of the given image using algorithm[3]. Apart from the ideal acquisition, we are using non-ideal acquisition to enhance the image. This method could give the required image and more suitable than the given image as input i.e. original image. The term spatial domain means working in the given space in this case the image it implies working with pixel values are in other words, working directly with the raw data.



Frequency domain: Image enhancement can be takes place by applying filters on the real image. The main usage of filters here to smoothen and sharpening of image appearance by removing very low and very high components. The change we observe for an whole image unlike enhancement in spatial domain. We are using two filters

(i) Low pass filter

(ii) High pass filter

Both type of filters that are using to keep high frequency and low frequency components of the image. In between these two filters to make smooth image we are using low pass filters whereas to sharpen the image can be done by high pass filters.

Spatial domain: It is the second method for enhancement technique of an image. The term spatial domain means working in the given space in this case the image it implies working with pixel values are in other words, working directly with the raw data.

$F(x,y) \rightarrow$ be the original image

Where, F is grey level value and (x.y) are image coordinates

For a 8-bit image 'F' can take values from 0 to 255 where '0' represents black , '255' represents white and all intermediate values represents shades of grey.

In an image as size 256x256, x and y can take values from (0,0) to (256,256).

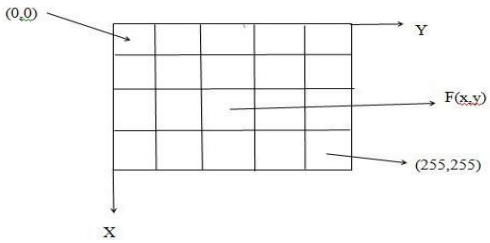


Fig 1.1 Spatial domain pixel analyze diagram

The above Fig 1.1 explain about the representation of F(x,y) of an image and modified image can be express as

$$G(x,y) = T[F(x,y]$$

Where F(x,y) is the original image

T is the transformation applied to get a new modified image G(x,y)

In between point processing, we are using point processing method in this project.

(A) Xilinx System Generator(XSG):

A model based approach that present in simulink/ matlab design where implementation into FPGA a DSP tool required and that is xilinx system generator(XSG). It extends the ability of simulink system level simulation environment. The main feature here is the FPGA fabric, different registers logic. XSG

besides the functional blocks of simulink library which included and used to develop the building blocks of DSP and any digital circuit. It is the computational system of the given input and decides the type of output generated for the given input as well as quantize the output. The system of DSP blocks those are converted to RTL easily by using this system generator. ISE tool helps to synthesize the design into xilinx's FPGA.

The combination of xilinx blocks, matlab and simulink blocks which create the test bench for analysis the data that produced in the model. XSG which simplifies the development of an algorithm and verification. The VHDL code using to work the functional block set and produces the output data for the user.

The DSP development flow of any design where the system model and its algorithm that can create in the simulink system, it then follows the given code accord execute and analysis the VHDL and cores of the design. ISE tool using to implementation of xilinx and that converts into bitstream finally it could be downloaded into FPGA board[4]. According to the simulation flow besides we have HDL test bench and test vectors that to examine the image that we have given as input and produced output.

II.LITERATUE SURVEY

R. Harinarayan, R. Pannereselvam, M. Mubarak Ali, D. Tripathi The new form of edge detection recognized. Primary or the fundamental feature of image is edge. Image processing ventures and computer classic vision feel that edge detection play important role. It is the first step towards the study and comprehension of images. To extract the information from digital aerial images with the continuous improvement of remote sensing images, particularly the appearance of digital aerial images edge detection consider the necessary step around it. The main aim of edge detection is to recognize the information in a picture about the shapes and the reflectance or transmission. The reliability and correctness of its outcomes directly impact on the understanding computer a structure made for a world of goals. The FPGA-based architecture which helps edge detection algorithms has been proposed in this paper. The use of embedded multipliers and massive memory are the benefit of the edge detection algorithms implementation on a field programmable gate array (FPGA). FPGAs provide a platform to process real-time algorithms with significantly higher performance on application-specific

hardware than programmable digital signal processors (DSPs). The proposed architecture can be used for navigation and pattern recognition as a building block of

aerial imaging systems. The results of the hardware implementation for the operator of Sobel and Prewitt are discussed.

A.Amaricai, O.Boncalo, M.Iordate, B.Marinescu A canny edge detection accelerator concept should be implemented on FPGA was proposed. The proposed architecture which relies on a 7-8 pixel moving window that performs the algorithm's more computationally complex operations: smoothing, calculating the magnitude and direction of the gradient, non-maximum suppression and double thresholding. Introductory outcomes are stored inside the FPGA by using the recommended window, without the need to buffer them into broad memory structures. In addition, due to its large number of pipeline levels, the design has a high throughput rate, facilitating substantial output for the proposed algorithm.

R. Dutta, K. Mitra, S. Mukherjee, and P. Sharma To define some very important problems the advanced architecture require and provide in the development, such as the identification of individuals and the counting of individual flows for security measures in restricted organizations. The aims are to continuously track activities in restricted regions to detect unnecessary congestions and forecast the movement of people to better control the density of crowds at the target site. This unique approach helps us as the device can sense the target object frame, detect the target's edges immediately, process the captured footage automatically and provide the filtered edition of the target image / video. Additionally, the motion of the target object (people) can also be monitored by our proposed method. Also color histograms (RGB) help us to make prompt decisions while capturing the total range of existing digital image/video.

III. BLOCK DIAGRAM OF SPARTAN 6 FPGA

The family of sprtan-6 provides leading integrated system capabilities along with lowest total cost for high volume applications. The density ranging from 3840 to 147443 logic cells which are expanded the power consumption almost half while comparing with other spartan family and faster, more comprehensive connectivity. It builts on a mature 45nm low power copper process technology and delivers the optimum balance of cost, power and performance. The spartan-6 family gives a new, dual register 6-input look up table(LUT) logic, more efficient and rich selection of built-in system level blocks. These include SDRAM memory controller, 18kb(2x9kb) block RAMs, enhanced mixed-mode clock management blocks ,..etc. These features available for a low cost programmable alternative to custom ASIC products with unprecedented ease of use spartan-6.

The best solution for high volume logic design is FPGA. The programmable silicon foundation to design targeted platforms which deliver integrated software and hardware that enable designers focus on innovation as soon as their development cycle begins are FPGAs. This spartan-6 FPGA board store the modified configuration data in SRAM type internal latches. The number of configuration bits are between 3Mb and 33Mb depending on device size and user design implementation options. Here the configuration storage is volatile in the nature and should be reloaded whenever the FPGA is powered up.

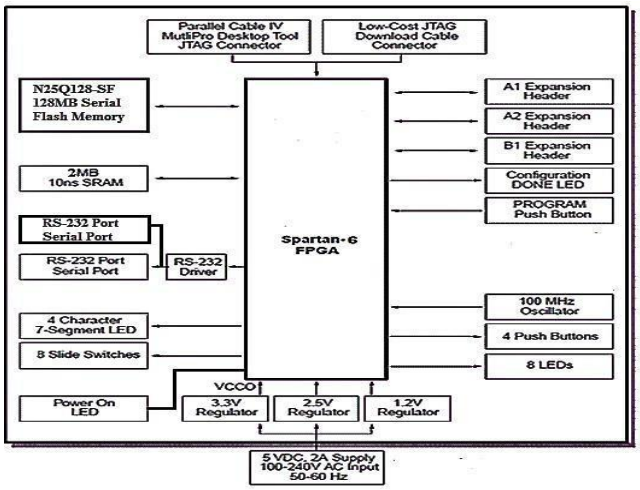


Fig 3.1FPGA spartan-6 block diagram

Flash ROM platform can reload this storage. The JTAG pins use boundary scan protocols to load bit configured data. The spartan-6 FPGA configures itself from a directly attached industry-standard SPI serial flash PROM.

Hardware used: Power regulators, power LED's, RS-232 connector, 8 slide switches, JTAG connectors, 7-segement display.

Software used: Matlab 2013b, xilinx ISE 14.7 simulator.

IV. DESIGN AND IMPLEMENTATION

In general paper algorithm the basic analysis for the piecewise linear transformation function where the pixel values directly compare and processing through it[5]. The blocks are xilinx blocks and we studied about the spatial domain which directly works on the pixel values of the image rather than frequency domain in the below figure 4.1 the selection of processing pixel values depending on the selection line exist in the diagram.

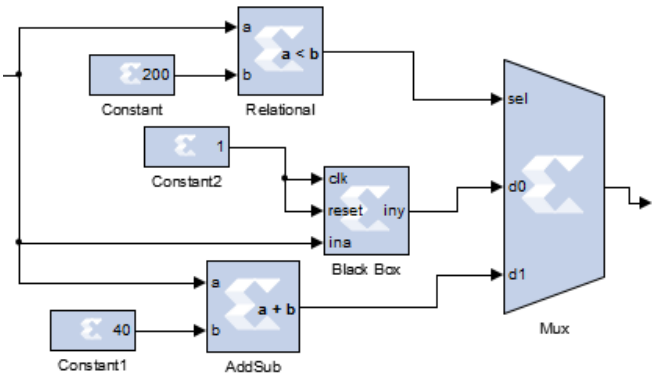


Fig 4 .1 Xilinx Block set

The relational block where the value of pixel is less than 200 as comparison present to the block and its selection line should be d0 otherwise it selects the d1 as given input to the Mux that are using.

Black Box: The programming of piecewise linear transformation by using VHDL. The total program file should be assign to the black box as well as to import the xilinx blocks into simulink we are using this box functionality.

In between d0 and d1 output of total functionality of basic piecewise linear transformation based on the clock that present ad corresponding Here the configuration storage is volatile in the nature and should be reloaded whenever outcome from the multiplexer(MUX).

The image acquisition takes place by the "image from file" exist in the simulink library. Here total analysis of the enhancement using point processing method of linear transformation technique and it is developing the matlab/simulink.In this piecewise linear piecewise linear transformation function where the pixel values directly compare and processing transformation the image that could be divide in to different areas i.e. pieces and examine those pixel values in the format of matrices. These pixels should send to the subsequent block present in the design.

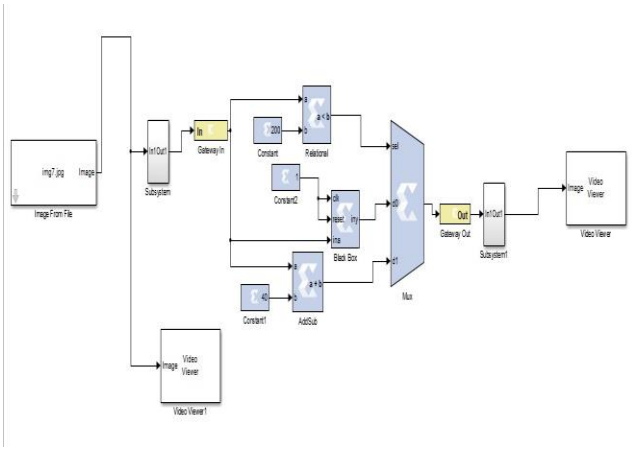


Fig 4.2 Piecewise linear transformation diagram in Simulink

The image which selected from the file later transmits through "subsystem" block whrer it converts into frames because each pixel of the image converts in the form of signal and send through the xilinx block set and these xilinx blocks input always in the form of 'bits' , to convert into bits or frames the comprising block subsystem using and transmits along "Gateway In" block in the figure.

Gateway Blocks: The establishment of connection from simulink blocks to xilinx blocks these blocks are used. As shown in the Fig 4.2 both sides of the gateway blocks (Gateway In, Gateway Out) are the signal conversion of input image pixels in front side as well as the output of multiplexer that needs to send from second end.

The enhanced image can view from the "Video Viewer" of the given input image simultaneously observe the input image from "Video Viewer1" as it present in the diagram.

The enhancement in the proposed architecture and make it into area efficient algorithm as well as reducing the complexity in the analysis we are using FPGA board. Among all we are using spartan-6 family to get the enhancement of given image. To assign the properties or features of "system generator" that consist three phase operation using xilinx blocks

1. Image pre-processing blocks
2. Contrast enhancement using XSG
3. Image post processing blocks

The detailed analysis of these operations as follows

Image pre-processing blocks:

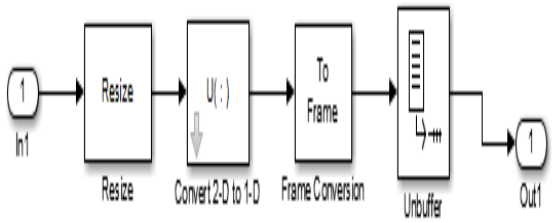


Fig 4.3 Pre-subsystem block diagram

The input image primary consideration is size of the image, the first step towards it can be resize the image accord to the configuration of the FPGA board. Whatever the size of the input image that should be sized into 256x256 and the image analysis in matrices form in that coverts into 1-D format, because here the pixel values of the image turns into frames or signal, finally unbuffer it and send through the block generated by the system generator which collaborated with FPGA board. To comprise these blocks we generate 'subsystem1' block.

Contrast enhancement using XSG: the base of enhancement here in the grey scale outcome of the image in that mode of operation initially we do contrast stretching which means darker portion more darker and bright portion more brighter. So the segregation lies in between 0 to 255 where '0' is black and '255' is white. To do this we use system generator block in simulink library.

To assign the 'system generator' properties in FPGA board i.e. spartan-6 FPGA we have to take from the simulink library as xilinx token, after allotment of clock frequency and FPGA spartan-6 we generate co-simulation block for design the image enhancement circuit. The FPGA generated block which comprises the xilinx block set and gateway blocks represent in Fig 4.2. The bitstream operation all could be done by the FPGA block.

Image post-processing blocks:

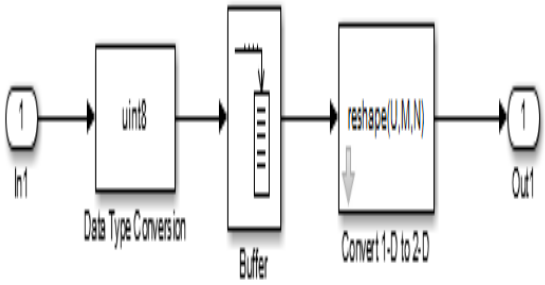


Fig 4.4 Post subsytem block diagram

The contradiction operation performed by these blocks present inth figure 4.4 where the data type conversion to send through the buffer and again reshape into the image for desired output of enhanced image. In this case signals needs to be converted in two dimentional format of the view of image taken place leads to enhanced it. To comprises that we produce “subsystem2” block. Finally it viewed from the “Video Viewer2” block present in the modified circuit of enhancement using FPGA.

FPGA Block circuit:

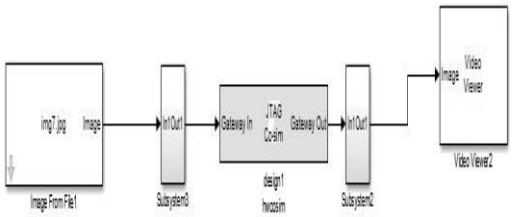


Fig 4.5 Hardware-software co simulation using spartan-6

The desired circuit of image enhancement using FPGA as shown in the above with help of spartan-6 family to get grey scale enhanced output of the original image and it is the modified circuit of Fig 4.2 where the gateway blocks collaborated with the xilinx block set present should be changed into one block of hardware software co-simulated block and it is generating by connecting spartan-6 FPGA using JTAG connector.

V.SIMULATION RESULTS

The algorithm using for contrast stretching should be implemented on matlab 2013b and Xilinx System Generator besides with spartan-6 FPGA that we get enhanced output image of the given image. The size of the image which convert always in 256x256 and resolution increasing at outcome of image. The enhancement results shown below

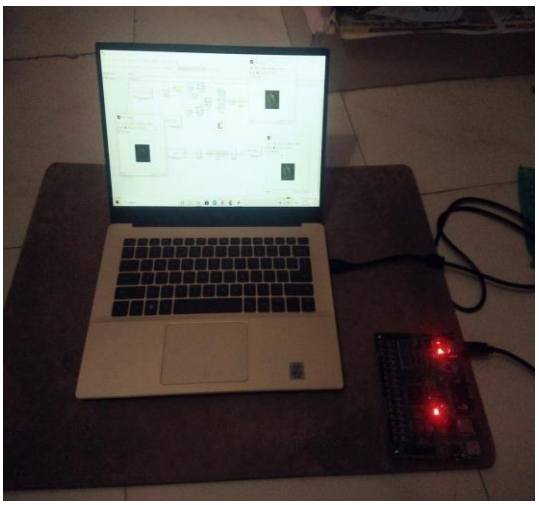
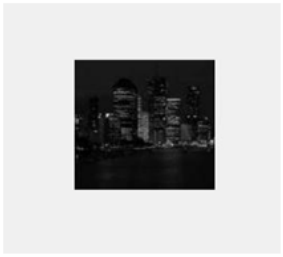
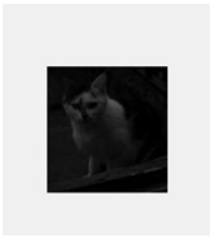


Fig 5.1 Execution using FPGA board



Input image



Input image

Fig 5.2 Desired result

The above all figures depicts the enhanced images of corresponding inputs given to the circuit designed to get enhanced output Fig 5.1 shows the enhanced image execution using spartan-6 FPGA board.

Table 1: Design Utilization

Logic Utilization	Used	Available	Utilization
Number of slice Registers	8	4800	0%
Number of slice LUTs	22	2400	0%
Number of fully used LUT FF pairs	8	22	36%
Number of bonded IOBs	17	102	16%

The algorithm proposed here found to be area efficient the number of slice registers used is 8 out of 4800.

CONCLUSION

The image processing algorithms are using in so many fields. The algorithm that developed in this project which relates the piecewise linear transformation with help of Matlab/Simulink with interfacing xilinx spartan-6 board any sort of image that converts into Grey scale image with enhanced ability of an image. In real time applications this project which help recognize the images that blur and not clear. For instance of licence plate recognition, vehicle detection and MRI application in medical ..etc. Later the piecewise linear transformation method can be implemented into FPGA.

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