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A Comprehensive Analysis of Low Power VLSI using CNTFET and GDI Technology

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***Abstract*—Low-power Very Large-Scale Integration (VLSI) using Carbon Nanotube Field-Effect Transistor (CNTFET) and Gate Diffusion Input (GDI) technology integrates nanomaterials for power consumption reduction. The CNTFET offers high-speed operation, while GDI minimizes transistor count and power consumption, making the model suitable for low-power applications. However, high power consumption and additional chip area occur due to inefficient circuit design and integration in low-power VLSI circuits using CNTFET and GDI technology. In this analysis, arithmetic and signal processing combinational circuits, are analyzed for low-power VLSI in CNTFET and GDI technology. In the arithmetic circuit, the full adder based on dynamic threshold, 6-transistor full adder, and in the signal processing unit, the 4-bit unary decoder and multiplexer are implemented in the combinational circuit. The power consumption, latency, PDP, and energy consumption are considered as the performance metrics of the methods.**

Keywords—arithmetic circuit, carbon nanotube field-effect transistor, gate diffusion input, power consumption, very large-scale integration.

I. Introduction

The enhancement of electronics over the past few decades has led to the development of advanced technologies that have transformed various aspects of modern society. Very Large-Scale Integration (VLSI) technology is crucial for minimizing power consumption, which helps maximize battery life with minimal heat generation due to excessive power consumption [1]. The cost of the entire system and the battery life are impacted by increased power consumption. The CNTFET provides increased elasticity to design high-performance circuits with low off-current. The CNTFET is a viable alternative to silicon-based transistors. An advantage of CNTFET is that it minimizes the amount of material required during the fabrication process [2]. The Gate Diffusion Input (GDI) cells in production offer full swing output with a low number of transistors, which results in reduced voltage drop. CNTFET technology has been employed with GDI, and the integration of CNTFET and GDI cells allows for the construction of smaller area designs [3].

Digital communication devices are used in applications such as video and image processing, microcontrollers, and digital signal processing, which perform various operations like subtraction, multiplication, and addition. The complexity of low power consumption is important for improving elaborate and sophisticated circuits such as the Arithmetic Logic Unit (ALU), which is a challenging component [4]. The ALU is utilized to determine the power consumption and area of a processor, and the full adder design used in the ALU enhances the performance of the arithmetic logic unit. CNTFETs are set to replace silicon-based transistors. In VLSI technology, power consumption parameters are essential [5]. The advantages of CNTFETs include minimizing the amount of material used during the fabrication process [6].

The remainder of this paper is presented in the following way: Section 2 provides a literature survey on the taxonomy of combinational circuits. Section 3 presents a comparative analysis of various existing models, while Section 4 discusses the challenges in low-power VLSI using CNTFET and GDI technology. Section 5 concludes the paper.

II. Taxonomy for Combinational Circuit

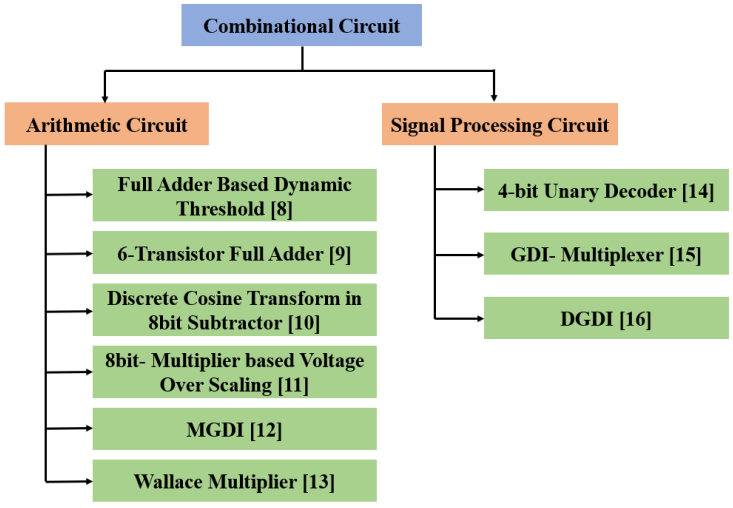

Fig. 1. Taxonomy for combinational Circuit

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Low-power VLSI using CNTFET and GDI technology is divided into the combinational circuit. The combinational circuit is further divided into arithmetic circuits and signal processing circuits for low-power VLSI. Figure 1 illustrates the taxonomy of the combinational circuit.

A. Arithmetic Circuit

An arithmetic circuit is a computational model used to accomplish arithmetic operations like division, multiplication, addition and subtraction on numbers. It consists of nodes representing variables, constants, and arithmetic operations, with edges connecting them to form a network of calculations. These circuits are designed to implement mathematical operations, often optimized for speed, power, or area efficiency.

Sadeghi et al. [7] developed a Dynamic Threshold technique with CNTFET technology utilized to achieve three new approximate Full Adders (FA) with the number of transistors being varied between 6 and 8. The FA was optimized through Nondominated Sorting based Genetic Algorithm II (NSGA-II), and features such as power delay, output swings and energy were extracted. The DT technique and FA circuits were directly utilized in error-tolerant applications, balancing the trade-off between the circuit and parameter accuracy. By using CNTFET and FA with 6 and 8 transistors, the circuit minimized power consumption due to reduced leakage currents. However, the FA circuits propagated to higher-level circuits, which led to error propagation and inaccuracies in larger systems.

Bahrami et al. [8] introduced an inexact 6-transistor FA based on GDI and DT approaches, which provided full swings output. The FA consisted of three errors and utilized a 10-transistor inexact 4:2 compressor based on stacking circuit data. A Sum of Block Differences block was presented through the FA and compressor. The SAD block was utilized for bioimage differentiation detection to identify brain strokes. The integration of GDI and DT approaches reduced the number of transistors and minimized switch activity, resulting in low power consumption. However, the GDI-based design suffered from limited drive strength, which led to performance degradation when the FA drives larger loads or more complex circuits.

Esmaeili et al. [9] implemented two 8-transistors approximate FA and subtractor, which were embedded into an 8-bit Ripple Carry Adder (RCA) and subtractor. The FA and subtractor were integrated into a multiplier-free DCT approach for compressing and eliminating noise in medical images. The FA and subtractor were embedded into the 8-bit RCA and 8-bit subtractor in the multiplier-free DCT. The 8-transistor DCT manipulation required only addition and no multiplication. This 8-transistor design significantly minimized hardware complexity, which improved area efficiency, a critical factor. Nevertheless, the RCA experienced high propagation delay due to its sequential nature, which reduced the speed of signal transitions because of the low transistor count.

Sadeghi et al. [10] implemented a Voltage Over Scaling (VOS)-based 8-bit multiplier using a high speed multiplier technique with 5:3 and 7:3 counters. The VOS minimized power consumption in digital circuits by adjusting voltage at various stages of the multiplier, which increased delay at various stages. To avoid threshold voltage drop in the GDI-based circuit, it was carefully tuned to achieve full-swing outputs with high driving capability. The VOS reduced the supply voltage below the nominal level, leading to significant power savings and improved power efficiency. However, the VOS introduced timing errors when the supply voltage was scaled down excessively, which caused unreliable performance.

Tyagi et al. [11] introduced an ultra-low-power 8-transistor MGDI-CNTFET FA that was evaluated in terms of propagation delay and power consumption at various power supply levels and temperatures. The MGDI-CNTFET-FA utilized a 10nm CNTFET model, where “10” carbon nanotubes were placed under the gate to conduct current from the source to the drain. The MGDI-CNTFET-based FA made use of the properties of CNTFET and MGDI logic style to minimize power consumption by reducing short-channel effects and lowering leakage currents. However, the CNTEFT provided high performance, but was sensitive to temperature variations, which led to performance degradation and temperature sensitivity.

Esmaeili et al. [12] developed a CNTFET-based FA that reduced power consumption, with the swing determined through DT technique. The FA design used 10 transistors, two internal nodes, and three errors, which were passed through the FA to minimize delay and dynamic power. The FA was utilized in three 4:2 compressors with 12, 16 and 20 transistors. A stacking technique was employed with the compressors to achieve low power consumption at a high speed with small area. The swing issue was addressed using DT techniques, which ensured appropriate output voltage levels and enhanced signal integrity.

B. Signal Processing Unit

A Signal Processing Unit is a specialized hardware component designed to process and manipulate various types of signals such as audio, video, or sensor data. It performs operations like filtering, transformation, and compression to enhance or analyze the signals. These circuits are often involved in signal conversion (digital to analog) and decoding operations, and offer versatile functionality in signal pathways, enabling performance efficiency.

Mujumdar et al. [13] developed a 4-bit unary weighted Current Steering digital to Analog Converter (CS-DAC) with minimal Integral Nonlinearity (INL) error for reduced power consumption and low glitch area. The input to the variational switch was handled by a thermometer decoder constructed using GDI. A unary decoder was utilized in the digital block of the CS-DAC to reduce space and power consumption. Unary weighting was used to minimize mismatch errors, specifically INL, which ensured high linearity in signal conversion. However, the design reduced glitch energy based on switching activity and layout symmetry, which led to minimized signal quality at higher operating speeds.

Shiri et al. [14] developed two FAs using Multiplexers (MUXs) and OR gates with GDI approaches. The cells were called GDI-based MUX approximate FAs, which included GMAFA1 and GMAFA2. The threshold voltage drop in GDI-based circuits was solved through CNTFET and DT approaches. The GDI approaches with multiplexers and OR gates helped in reducing power consumption. However, while the GDI minimized power consumption, it required additional transistors for multiplexers, which led to potential area overhead in the chip area.

Ghorbani et al. [15] introduced a low power FA-based model, integrated with dynamic logic style and GDI low power technique using the CNTFET. The dynamic logic style consisted of basic logic circuits like XOR and XNOR gates which resulted in full swing FA in CNTFET technology. The dynamic logic style and GDI helped achieve faster switching speeds which allowed for faster evaluation of the circuit's output. The swing issue was determined through DT techniques which ensured appropriate voltage output levels and enhanced the signal integrity. Nevertheless, the GDI technique minimized the number of transistors, but the CNTFET-based FA design occupied a larger area for integration which enhanced area usage.

III. Comparative Analysis

The low power VLSI using CNTFET and GDI technology is compared with existing methods to assess and enhance its performance. Table 1 presents the comparative analysis of existing methods.

TABLE I. COMPARATIVE ANALYSIS OF LOW POWER VLSI USING CNTFET AND GDI TECHNOLOGY

Author Name	Methodology	Circuit Name	Performance Metrics	Takeaways	Tools
Sadeghi et al. [7]	Dynamic Threshold and CNTFET technology	Arithmetic Circuit	Average power consumption (μW), Maximum propagation delay	Reduced circuit area, Improved power efficiency	Hierarchical Simulation Program with Integrated Circuit Emphasis (HSPICE), MATLAB
Bahrami et al. [8]	inexact 6 transistor FA depend on GDI and DT approaches	Arithmetic Circuit	average power, Power-Delay-product (PDP), Peak Signal-to-Noise Ratio (PSNR)	Area and power savings, error tolerance, high efficiency	Stacking Circuit Concept, Synopsys HSPICE-H-2013
Esmaeili et al. [9]	Two 8 transistors estimated FA and subtractor were embedded into 8-bit RCA and 8-bit subtractor	Arithmetic Circuit	PDP, PSNR	Power performance, small area and fast circuits, Reduced computational complexity	HSPICE Simulation tool, 32 nm Technology Node
Esmaeili et al. [12]	Ultra-power 8 transistor MGDI – CNTFET- FA	Arithmetic Circuit	partial product reduction tree (PPRT), normalized mean error distance (NMED), PSNR	High efficiency with imprecision, power area and efficiency	DCT, Full adder, Wallace Multiplier, HSPICE
Mujumdar et al. [13]	4-bit unary weighted CS-DAC with minimal INL error	Signal Processing Unit	Latency, power conumption and PDP	Low power consumption, high speed performance and area efficiency	HSPICE, Current Steering DAC, CNTFET and GDI
Shiri et al. [14]	Two FA proposed through Multiplexers (MUXs) and OR gates with GDI approaches	Signal Processing Unit	Error Distance (ED), NMED and PSNR	Smaller area Consumption, High speed performance for multistage system.	HSPICE, Full adders and MATLAB
Sadegh et al. [16]	AC-based Full Adder	Arithmetic Circuit	PDP, energy-delay-product (EDP) and power-delay-area-product (PDAP)	High speed performance, smaller area and energy efficiency	GDI, CNTFET and SPICE
Anjaneyulu and Reddy [17]	Full-swing 11 Transistor (11T) adder based on CNTFET	Arithmetic Circuit	Delay and PDP	Improved power and low power	SPICE, CNTEFT
Mahania and Keshavarzian [18]	High-speed 1-bit FA cells	Arithmetic Circuit	Power consumption, propagation delay, energy consumption and EDP	Energy efficiency, low power delay product and high speed	HSPICE
Tyagi et al. [19]	10-T CNTFET full adder with GDI technique and 10-T Finfet based full adder using GDI technique	Arithmetic Circuit	PDP, Power Consumption	Reduced Transistor Count, Application in Low-Power, High-Performance Systems.	10-T CNTFET full adder and SPICE

IV. Problem Statement

The problems identified from recent research analytics of low power VLSIs using CNTFET and GDI technology are described in this section. Table 2 represents the problem statement of low power VLSI using CNTFET and GDI technology.

TABLE II. PROBLEM STATEMENT OF LOW POWER VLSIS WITH CNTFET AND GDI

Problem	Description
High power consumption	High-power consumption stood as a challenge as the enhanced device scaling and high operating frequencies led to reduced battery life capabilities and reliability concerns.
Large area	Larger area utilization frequently led to increased chip size, power consumption, and slower performance due to longer interconnections and higher capacitance.

V. Conclusion

Low Power VLSI using CNTFET and GDI technology focuses on designing energy-efficient circuits by exploiting the high-speed and low-power characteristics of CNTFET, along with the minimal transistor count and reduced power consumption of GDI logic. In this analysis, both the arithmetic circuit and signal processing circuit are considered as combinational circuits for low-power VLSI design using CNTFET and GDI technology. This integration enables high-performance, low-power systems for next-generation digital circuits. This study presents the combinational circuit, which is divided into arithmetic circuit and signal processing units for low power consumption and area efficiency. The circuits such as FA, DGI, DCT, MUX and RCA are analysed to determine the best balance between low power consumption and area efficiency. Additionally, tools like Stacking Circuit

Concept, HSPICE and Current Steering DAC are used to estimate the performance of the model. Power consumption, latency, PDP and energy consumption are considered the key performance indicators for these methods.

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