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MODELING AND ANALYSIS OF THRESHOLD VOLTAGE FOR DUAL-HALO DUAL-DIELECTRIC TRIPLE-MATERIAL SURROUNDING-GATE METAL–OXIDE–SEMICONDUCTOR FIELD-EFFECT TRANSISTORS

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Abstract- An analytical model of threshold voltage for a Dual-Halo Dual -Dielectric Triple-Material surrounding-gate (DH-DD-TM-SG) MOSFET is presented. The model described in this paper also incorporates the effect on threshold voltage with variation in silicon film thickness and gate oxide thickness. Moreover the consequence of variations in device parameters like drain bias, gate length ratio, radius of silicon pillar and channel doping concentration are also inspected. A comparison is made between the performance of TM-SG MOSFET and proposed device. A significant improvement has been observed in DH-DD-TM-SG MOSFET structure which can be used to make system-on-chip devices. The effectiveness of the developed model is closely agree with the TCAD results confirms the validity of the proposed model.

Index terms*:* Threshold Voltage, Halo Implant, Gate Stack, Oxide Thickness, Surrounding Gate MOSFETs.

I. INTRODUCTION

The mobile and computing markets continue to innovate at a dramatic rate delivering more and more performance in smaller and smaller form factors with higher and higher power efficiencies. One of the keys to enabling this is the semiconductor technology that provides the platform for building the system on a chip (SoC) components at the heart of these devices. The underlying transistor technology most SoCs are built on today uses the planar MOSFET transistor. One of the major challenges with scaling planar MOSFETs over recent process technology generations has been in delivering on the switching speeds in large SoCs at reduced power consumption levels. One of the key limitations impacting power in planar MOSFETs is the short channel effects and in particular the "off-state" leakage current which increases the idle power unnecessarily. In view of difficulties of the planar MOSFET technology to get the acceptable gate control over the channel multiple gate based devices is better technology option for further shrinking the size of the planar MOSFET [1-4]. Finally, a viable solution has emerged, the Multigate devices. This evolution of the MOSFET has proven to be the best choice for next generation processes but brings with it some

new challenges for manufacturing and design that require careful consideration if the benefits with Multigate devices can be capitalized on.
Auth et. al. proposed a threshold model for surrounding-gate MOSFETs. The threshold voltage for the device is equal to perimeter weighted sum of the threshold voltages. This is only used for the non-gate engineered structures of surrounding gate MOSFETs [5]. Kumar et. al. has presented a new analytical model for the threshold voltage of a dual-material surrounding-gate MOSFETs. The model results accurately predict the threshold-voltage roll-off for channel lengths even less than 90nm [6]. Tiwari et. al. proposed a 2-D analytical model for threshold voltage of TM-DG MOSFET. The effects of device parameters on the threshold voltage are discussed and the results are analyzed [7]. Wang et. al. is described a mathematical model for the surface potential and threshold voltage of TM-SG MOSFETs to investigate short channel effects. The paper used superposition method and Bessel functions method to find the threshold voltage of the device. The method uses some complex expression and mathematical calculations [8]. The threshold voltage model of TM-SG MOSFETs has been proposed by P.S. Dhanaselvam et. al. But model is not adequate for DH-DD-TM-SG MOSFETs [9-10].

II. MODEL FORMULATION

Figure 1 shows the schematic diagram of DH-DD-TM-CGAA MOSFET structure. The figure shows that the gate terminal consists of three metals with different work functions for cylindrical surrounding gate MOSFET. In this Triple metal gate schematic, the symmetric dual halo doping is incorporated for the first time along with dual dielectric to form a novel device structure. The lengths L_1 and L_5–L_4 are halo doped with concentration N_{dh} while the rest of the regions are doped with acceptor doping concentration N_{ak}, assuming that N_{dh} is greater than N_{ak} [11].

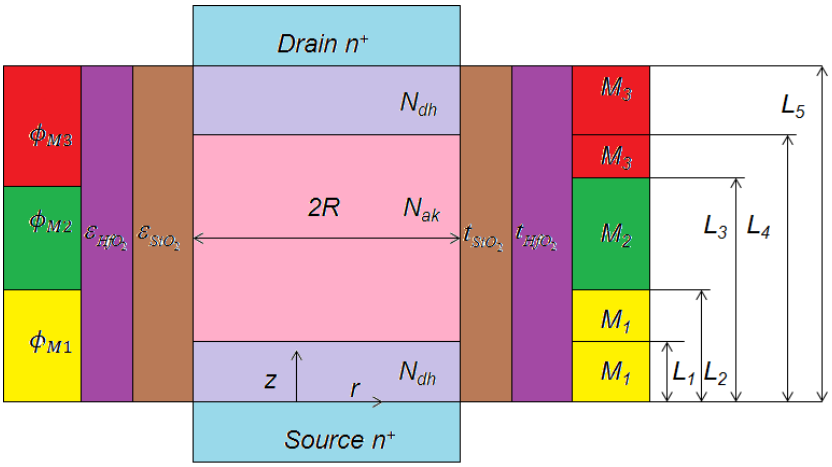

Figure 1. Cross sectional schematic of Dual-halo dual-dielectric triple-material surrounding-gate MOSFET

2.1. SURFACE POTENTIAL MODELING

The cylindrical coordinate system is a radial direction *r*, an angular direction θ in the radial plane, and a vertical z, as mentioned in Fig 1. The surface potential and the field vary with r and z, but not with θ with respect to the structural symmetry of the device. So 2-D analysis is needed.

The potential distribution in the channel can be expressed by the Poisson's equation and can be written as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial[\phi_k(r,z)]}{\partial r}\right)+\frac{\partial^2[\phi_k(r,z)]}{\partial z^2}=\frac{qN_{ak}}{\varepsilon_{Si}} \quad (L_{k-1}\le z\le L_k) \qquad (1)$$

Where k=1, 2, 3, 4, 5

$$\phi(r,z)=\begin{cases}\phi_1(r,z);0\le z\le L_1\\ \phi_2(r,z);\mathrm{L}_1\le z\le L_2\\ \phi_3(r,z);\mathrm{L}_2\le z\le L_3\\ \phi_4(r,z);\mathrm{L}_3\le z\le L_4\\ \phi_5(r,z);\mathrm{L}_4\le z\le L_5\end{cases} \qquad (2)$$

The potential distribution is approximated using parabolic profile for DHDDTMCGAA MOSFET in the radial direction and is given by [10].

$$\phi(r,z)=\zeta_0(z)+\zeta_1(z)\mathrm{r}+\zeta_2(z)\mathrm{r}^2 \qquad (3)$$

Where the constant $\zeta_0(z),\zeta_1(z)$ and $\zeta_2(z)$ can be attained by substituting conditions at the boundary.

For obtaining surface potential, the corresponding boundary conditions are:

(1) Surface potential $\phi_s(z)$ depends on z only

$$\phi(\mathrm{R},z)=\phi_s(z) \qquad (4)$$

(2) The center potential $\phi_c(z)$ depends on z only

$$\phi(0,z)=\phi_c(z)=\zeta_0(z) \qquad (5)$$

(3) The metal gates have continuous electric flux at the interfaces of the gates/oxide. Therefore,

$$\left.\frac{d\phi_k(r,z)}{dr}\right|_{r=R}=\frac{C_{oxeffdh}}{\varepsilon_{Si}}(\mathrm{v}_{gs}-\phi_{sk}(z)-\mathrm{v}_{fbk})=2R\zeta_2(z) \qquad (6)$$

Where k=1, 2, 3, 4

$C_{oxeffdh}$ is the effective gate oxide capacitance for DH-DD-TM-SG MOSFET [12].

$$C_{oxeffdh} = \frac{\varepsilon_{SiO_2}}{R\ln\left[1+\frac{t_{oxeffdh}}{R}\right]} \quad (7)$$

Where $t_{oxeffdh}$ is the effective gate oxide thickness for DH-DD-TM-SGAA MOSFET [13].

$$t_{oxeffdh} = t_{SiO_2} + \frac{\varepsilon_{SiO_2}}{\varepsilon_{HfO_2}} t_{HfO_2} \quad (8)$$

Using the boundary condition equations [(4)-(8)] in the surface potential equation (3) and then substituting in equation (1).

Surface potential is expressed as

$$\frac{d^2\phi_s(z)}{dz^2} - \phi_s(z)\left(\frac{2C_{oxeffdh}}{\varepsilon_{Si}R}\right) + (\mathrm{v}_{gs} - \mathrm{v}_{fbk})\left(\frac{2C_{oxeffdh}}{\varepsilon_{Si}R}\right) = \frac{qN_{ak}}{\varepsilon_{Si}} \quad (9)$$

$$\frac{d^2\phi_s(z)}{dz^2} - \kappa^2\phi_s(z) = \chi \quad (10)$$

Where $\kappa^2 = \frac{2C_{oxeffdh}}{\varepsilon_{Si}R}$

$$\chi = \frac{qN_{ak}}{\varepsilon_{Si}} - \kappa^2(\mathrm{v}_{gs} - \mathrm{v}_{fbk})$$

Surface potential for all five regions are given as

$$\frac{d^2\phi_{sk}(z)}{dz^2} - \kappa^2\phi_{sk}(z) = \chi_k \qquad l_{k-1} \le \mathrm{z} \le l_k \quad (11)$$

$$\chi_k = \frac{qN_{ak}}{\varepsilon_{Si}} - \kappa^2(\mathrm{v}_{gs} - \mathrm{v}_{fbk}) \quad (12)$$

Where k=1, 2, 3, 4, 5

$$\mathrm{v}_{fbj} = \phi_{mj} - \left\{\chi_s + E_g - q\phi_{fp}\right\} \quad (13)$$

Where j=1, 2, 3, 4, 5

$$\phi_{fp} = \frac{KT}{q}\ln\left(\frac{N_{ak}}{n_i}\right) \quad (14)$$

The solution of second order differential equation (10), through the complementary and the particular integral functions is given as

$$\phi_{si}(z) = \alpha_k e^{(\kappa z)} + \beta_k e^{(-\kappa z)} - \frac{\chi_k}{\kappa^2} \qquad l_{k-1} \le z \le l_k$$

$$M_k = \frac{\chi_k}{\kappa^2} \tag{15}$$

$$\delta_k = \exp(\kappa L_k)$$

$$\delta_k^{-1} = \exp(-\kappa L_k)$$

Where α_k & β_k are arbitrary constants, which are calculated with the help of continuity conditions for the surface potential distribution (ϕ) and the field distribution (E) at the interfaces of different metal gates [14-15].

(1)The potential ϕ_{s1} , at the source end is given by

$$\phi_{s1}(z)\big|_{z=0} = V_{b1} \tag{16}$$

$$V_{b1} = \frac{KT}{q} \ln\left(\frac{N_{a1} N_d}{n_i^2}\right) \tag{17}$$

(2)The potential ϕ_{s5}, at the drain end is given by

$$\phi_{s5}(z)\big|_{z=l} = V_{b5} + V_{ds} \tag{18}$$

$$V_{b5} = \frac{KT}{q} \ln\left(\frac{N_{a5} N_d}{n_i^2}\right) \tag{19}$$

(3)The surface potential ϕ is continuous functions at the interfaces of different metal gates and can be written as

$$\phi_{sk}(z)\big|_{z=l_k} = \phi_{s(k+1)}(z)\big|_{z=l_k} \tag{20}$$

k=1, 2, 3 & 4

(4)The electric fields E are continuous functions at the interfaces of dissimilar metal gates and can be written as

$$\left.\frac{d\left[\phi_{sk}(z)\right]}{dz}\right|_{z=l_k} = \left.\frac{d\left[\phi_{s(k+1)}(z)\right]}{dz}\right|_{z=l_k} \tag{21}$$

k=1, 2, 3 & 4

For the value of α_k & β_k (k=1, 2, 3, 4 & 5), see **Appendix A**

2.3. MINIMUM SURFACE POTENTIAL MODELING

Differentiating surface potential equation (15) relative to the direction z and making it zero for getting the minimum surface potential $\phi_{s1\min}$.

$$\left.\frac{d\phi_{s1}(z)}{dz}\right|_{Z_{\min}} = 0$$

$$\phi_{s1\min} = 2\sqrt{\alpha_1\beta_1} - \frac{\chi_1}{\kappa^2} \tag{22}$$

2.4. THRESHOLD VOLTAGE MODELING

The device turn ON voltage is threshold voltage which is twice the Fermi potential and equal to minimum surface potential [7-8, 16].

$$\phi_{s1\min} = 2\phi_f$$

$$2\sqrt{\alpha_1\beta_1} - \frac{\chi_1}{\kappa^2} = 2\frac{KT}{q}\ln\left(\frac{N_{ak}}{n_i}\right)\Bigg|_{V_{gs}=V_{th}} \tag{23}$$

III. RESULTS AND DISCUSSION

The present analysis is carried out for surface potential ϕ_s and threshold voltage v_{th}. Simulation parameters are: V_{gs}=0.2V, V_{ds}=0.1V, R=10nm, $t_{oxeffdh}$=2 nm, $N_{dh}=10^{18}$ cm^{-3}, $N_{ak}=10^{17}$ cm^{-3}, $N_d=10^{20}$ cm^{-3}, L=50nm.

The threshold voltage of DH-DD-TM-CGAA MOSFETs is determined with respect to various device parameters and analyzed. In this TMG structure three dissimilar metal gate electrodes are utilized with disparate work function. The first screening gate has the moderate work function and the second screening gates adjacent to drain have the lowest work function. The control gate adjacent to the source has the highest work function.

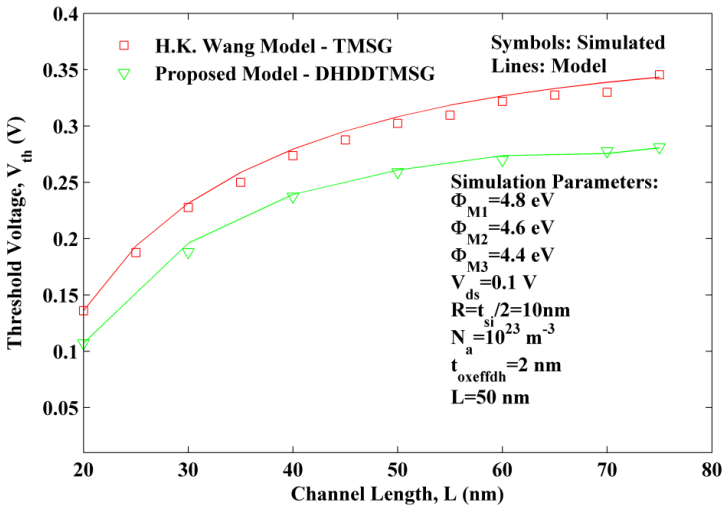

Figure 2. Depicts the deviation in threshold voltage with channel length for TM-SG and DH-DD-TM-SG MOSFETs

The threshold voltage of TM-SG and DH-DD-TM-SG MOSFET is compared in figure 2. From the figure, at lower channel lengths the threshold voltage roll-off is observed which shows the reduction in short channel effects. DH-DD-TM-SG has a less threshold voltage in comparison to TM-SG devices owing to improved gate controllability. Thus, the Dual-Halo Dual -Dielectric Triple-Material surrounding-gate/ cylindrical gate all around MOSFET are suitable for low voltage applications. From the plot, it is illustrated that the threshold voltage decreases swiftly when channel length reduces. This is mainly due to the control of gate electrode decline deliberately with increase in drain bias. It indicates starting of DIBL.

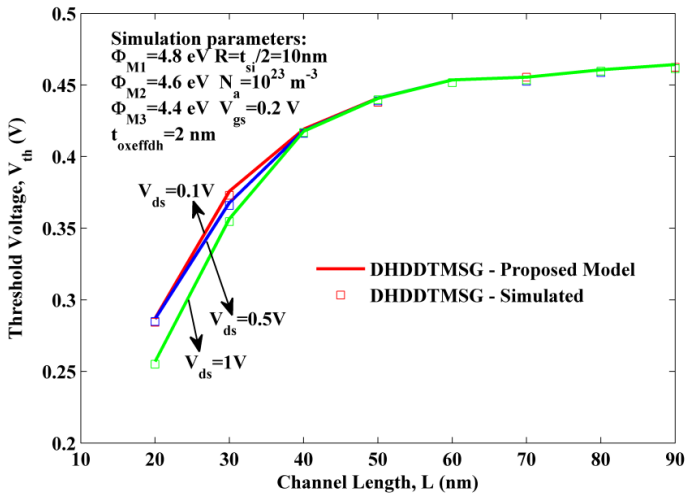

Figure 3. Deviation in threshold voltage with channel length at various drain voltages of V_{DS} 0.1, 0.5, and 1V

The increase in V_{DS} results in reduction in threshold voltage. Compared to TM-SG MOSFETs, the threshold voltage is lowered and shows better performance.

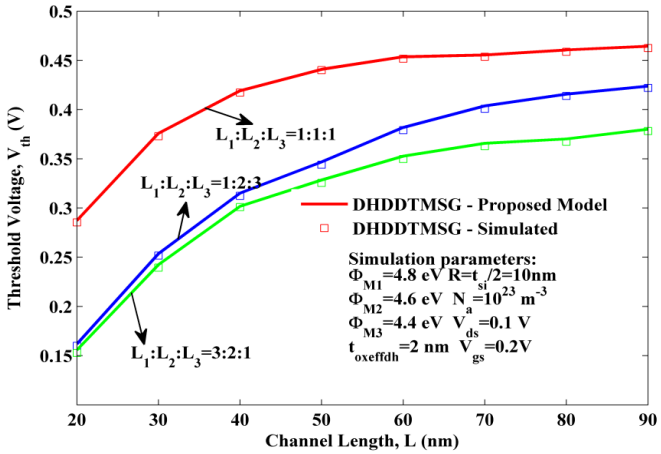

Figure 4. Shows the deviation in threshold voltage with channel length at various gate length ratios

The plot of threshold voltage of MOSFET versus channel length at different gate lengths. Higher gate length ratio is not suitable for low power applications as it yields a higher threshold voltage and reduces the threshold roll over when channel length is reduced .Also lower gate length ratio yields lesser threshold voltage. The gate length changes the proportion of gate materials which simultaneously varies the work function difference which varies the threshold voltage. The power dissipation will get increased with the higher gate length. As we increase the ratios of the lengths of screen gates, the threshold voltage will decreases. The distribution of electric field in the channel causes the variation of drain potential screening on the source side. Due to this variation, the barrier modulation on the source channel side gets decreased. Therefore, the Drain Induced barrier Lowering (DIBL) get decreased also reducing the V_{th} roll –off .the device is suitable for nanoscale applications only for lesser gate length ratios.

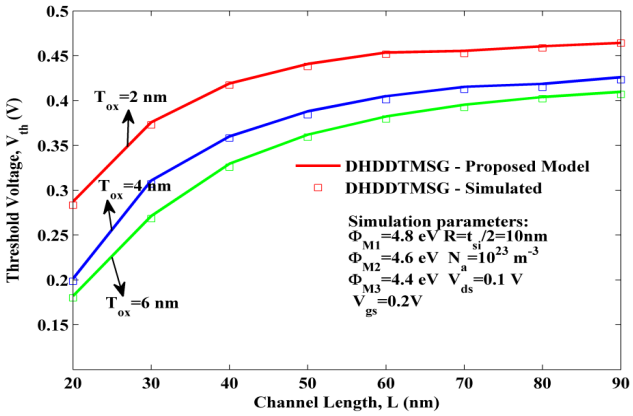

Figure 5. Shows the deviation in threshold voltage with channel length at various oxide thickness

It has been noticed that the oxide thickness is inversely proportional to the threshold voltage. It is observed that for the oxide thickness of 2nm, the threshold voltage is high. The thinner oxide layer produces the leakage currents in the sub threshold conduction. It is good to have optimum value of oxide thickness for reducing the leakage current and short channel effects.

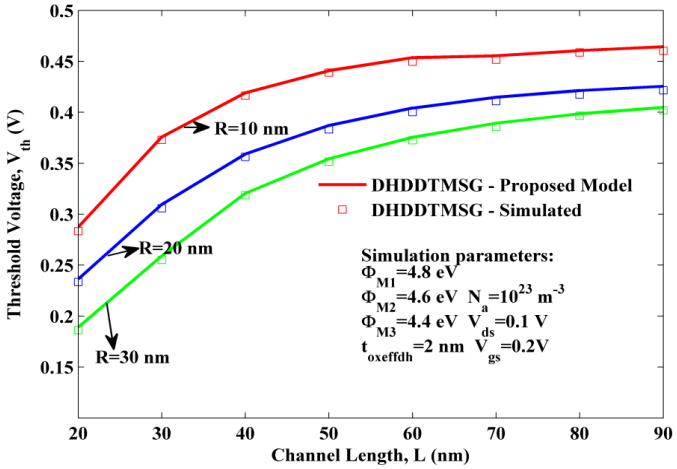

Figure 6. Shows the deviation in threshold voltage with channel length at various silicon thickness

Above figure shows the non-linear variation of threshold voltage w.r.t channel thickness. It is noticed out from the result that the threshold voltage bear an inversely proportional relation with the silicon thickness. The control of drain gets increased over the channel carrier while the control of gate electrode gets decreased over the channel. As the channel thickness increases over the drain, the threshold voltage gets decreased. The large threshold voltage also produces short channel effects making the device not suitable for low power applications. The analytical modeling results are validated with the TCAD simulation results [17].

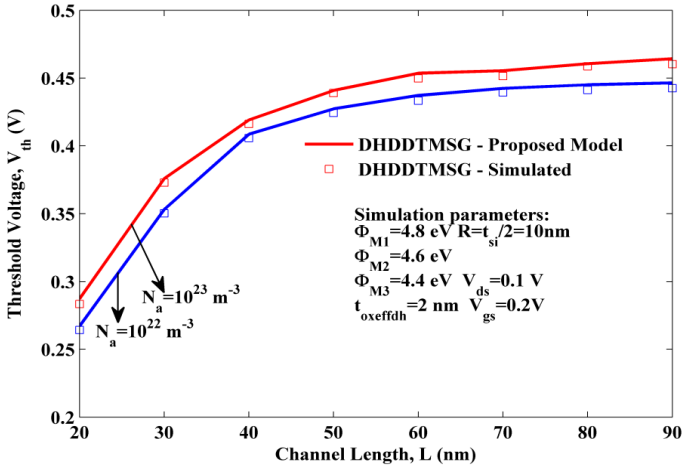

Figure 7. Shows the deviation in threshold voltage with channel length at various channel doping concentration

As the channel doping concentration increases, the threshold voltage is also increases. The barrier height is increased with varying channel doping concentration. Hence the voltage necessary to deplete the charge carriers is also increased. The analytical model results are compared with the TCAD simulation results and it is very closely related.

IV. CONCLUSION

In this paper, a 2-D analytical model for the novel device DH-DD-TM-CGAA MOSFET has been developed by using parabolic approximation. The analytical model for the surface potential and threshold voltage has been developed. The threshold voltage is observed for various device parameters like oxide thickness, silicon thickness, gate length ratios, doping concentration. It further studies the impact on the SCEs of the DH-DD-TM-SG MOSFETs with varying device parameters. It is shown that this proposed surrounding gate MOSFET having better performance as compared to existing TM-SG in suppression of SCEs.

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Appendix A

$$\alpha_1 = \alpha_5 + \frac{(M_4 - M_5)}{2\delta_4} + \frac{(M_3 - M_4)}{2\delta_3} + \frac{(M_2 - M_3)}{2\delta_2} + \frac{(M_1 - M_2)}{2\delta_1}$$

$$\alpha_2 = \alpha_1 - \frac{(M_1 - M_2)}{2\delta_1}$$

$$\alpha_3 = \alpha_2 - \frac{(M_2 - M_3)}{2\delta_2}$$

$$\alpha_4 = \alpha_3 - \frac{(M_3 - M_4)}{2\delta_3}$$

$$\alpha_5 = \frac{\left((M_1 - M_2)\delta_1 + (M_2 - M_3)\delta_2 + (M_3 - M_4)\delta_3 + (M_4 - M_5)\delta_4 - 2M_1 - 2V_{bi} + 2(M_5 + V_{bi} + V_{ds})\delta + \alpha_1\right)}{\left(2\left(-1 + \delta^2\right)\right)}$$

$$\beta_1 = \frac{(M_1 - M_2)\delta_1}{2} + \frac{(M_2 - M_3)\delta_2}{2} + \frac{(M_3 - M_4)\delta_3}{2} + \frac{(M_4 - M_5)\delta_4}{2} - \alpha_5\delta^2 + (M_5 + V_{bi} + V_{ds})\delta$$

$$\beta_2 = \beta_1 - \frac{(M_1 - M_2)\delta_1}{2}$$

$$\beta_3 = \beta_2 - \frac{(M_2 - M_3)\delta_2}{2}$$

$$\beta_4 = \beta_3 - \frac{(M_3 - M_4)\delta_3}{2}$$
$$\beta_5 = \beta_4 - \frac{(M_4 - M_5)\delta_4}{2}$$